Design and Integration of A Single-chip CMOS Transceiver for Passive UHF RFID Readers

by

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This is to certify that I have examined the above PhD thesis
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Abstract

In this thesis, a single-chip CMOS UHF RFID reader is implemented for passive RFID systems operated in 860MHz to 960MHz, which integrates a RF transceiver including IQ data converters and digital baseband.

Firstly, the distinctive features of RFID systems are analyzed, system and building block specifications are derived based on the EPCglobal Gen-2 standard. It is revealed that key challenges in implementing the RFID reader are self-interference caused by simultaneous transmitting and receiving at the same carrier frequency, as well as reconfigurability for multi-protocol operation. The goal of this project is to build systems that support multiple standards with multiple data rates and multiple modulation formats in different electromagnetic environment by a flexible system architecture.

As one of the critical building blocks, a low power low phase noise fractional-N frequency synthesizer is proposed. By properly distributing the capacitance between

drain and source of a transformer-feedback VCO, the modified VCO exhibits enhancement in tank Q factor, as well as benefits from the noise filtering of even harmonics. A 3rd order 2-bit single-loop ΣΔ modulator is optimized for the proposed synthesizer so that it achieves the optimization of phase noise and power consumption at the architecture level. In addition, the detailed design consideration, circuit implementation and theoretical analysis for a power-optimized reconfigurable baseband are presented, which is crucial for a multi-protocol RFID reader. It allows power optimization for different system bandwidth and interference scenarios.

Fabricated in 0.18μm CMOS technology, the proposed RFID reader occupies a chip area of 18.8mm^2. The synthesizer achieves the phase noise of –76dBc/Hz in-band and –126dBc/Hz at 1-MHz offset with a reference spur of –84dBc. For the listen mode operation with LNA turned on, the RX front-end measures P-1dB of –9.4dBm and IIP3 of 0dBm. The worst-case RX sensitivity is –90dBm for an output SNR of 11dB for all the bandwidths from 80 KHz to 1 MHz. In the talk mode with LNA bypassed, the RX front-end measures P-1dB of 3.5dBm, IIP3 of 18dBm. RX sensitivity is –70dBm in the presence of –5dBm self-interferer. The TX achieves output P-1dB of 10.4dBm and sideband rejection ratio of –53.6dBc. With maximum interference rejection ability, RX baseband power can be dynamically optimized from 63mW at 640kbps to around 6.2mW at 40kbps. It corresponds to a total RX power of 105.6mW to 47.8mW. The proposed RFID reader dissipates a maximum power of 249mW when transmitting maximum output power of 10.4dBm and receiving the tag's response of –70dBm in the presence of –5dBm self-interferer.

Chapter 1
INTRODUCTION

1.1 Introduction to RFID System

1.1.1 RFID Systems Overview

In recent years automatic identification procedures (Auto-ID) have been very popular in many service industries, such as purchasing and distribution logistics, manufacturing companies, warehouse management, passport and animal identification, etc. The prevalent barcode labels nowadays are found to be inadequate in an increasing number of cases. Barcodes may be extremely cheap, but their stumbling block is their low storage capacity and the fact that they cannot be reprogrammed and their operation requires a direct line-of-sight.

One potential solution is the radio frequency identification (RFID). This is an electronic tagging technology that allows an object, place, or person to be automatically identified at a distance using an electromagnetic challenge and response exchange. The information is stored in the tags which consist of a microchip connected to an antenna. In passive RFID systems, readers (interrogators) generate signals that are dual purpose: they provide power for a tag (transponders), and they create an interrogation signal. A tag captures the energy it receives from a reader to supply its own power and then executes commands sent by the reader.

Through the communication with readers, identification code stored in the tag can be made available to accessible databases to determine its identity. Such passive RFID system has the potential of extremely low cost, data transfer robustness, efficiency and high throughput. Fig. 1.1 shows the main components in an RFID system: a host, network, multiple readers and tags, the channel through which the reader and tags communicate.

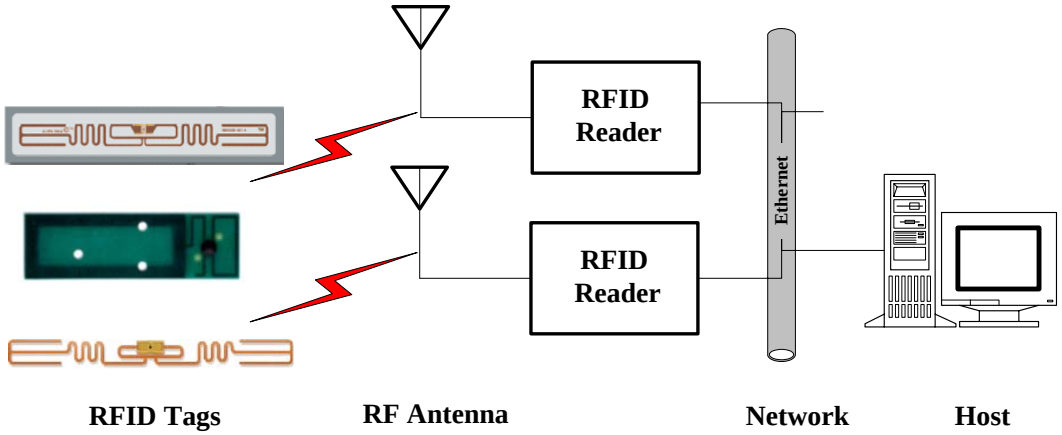
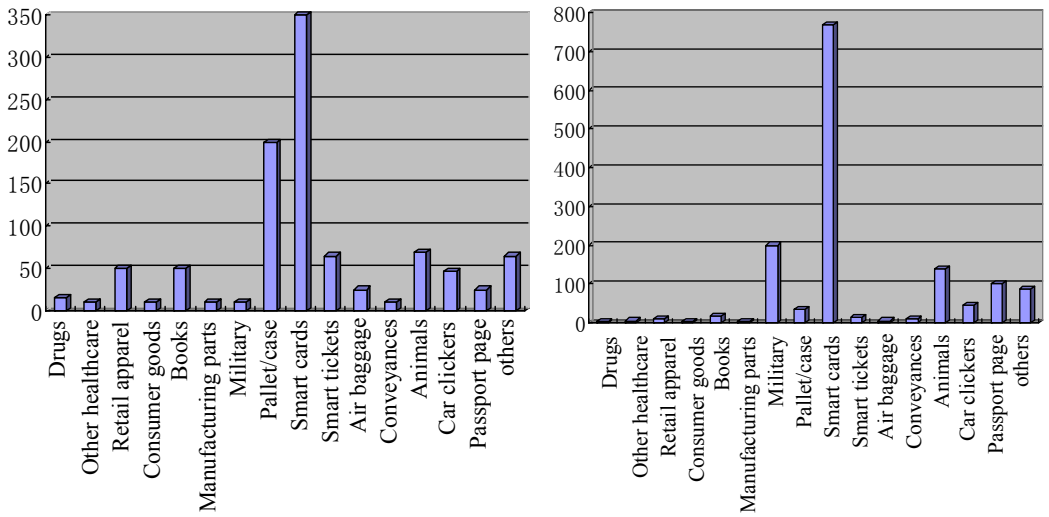


Fig. 1.1 Main components of an RFID system

With the maturity of technology and development of circuit design techniques, RFID is now making a splash, after its 40 years invention. It is known as military identification friend or for (IFF) systems that appeared during the Second World War. It is reported that at the start of 2007, the cumulative number of RFID tags sold over the last 60 years is 3.752 billion. 27% of that number was sold in 2006 and 19% in 2005, showing a very robust increase in sale. Fig. 1.2(a) shows the number of RFID tags sold in 2006. By far the most prevalent application of RFID is smart cards with a total number of 350 millions. Fig. 1.2(b) shows the tag market value in 2006. Again, smart cards with total value of 770 millions USD are the biggest segment. In 2007,

IDTechEx expect that 1.71 billion tags will be sold. The total RFID market value (including all hardware, systems, integration etc) across all countries will be $4.96 Billion.



(a) (b)

Fig. 1.2 (a) Number of RFID tags supplied in 2006 (millions) (b) total value spent on RFID tags in 2006 (USD $ millions)

(Source: IDTechEx RFID Forecasts, Players and Opportunities 2007-2017 www.idtechex.com/forecasts)

1.1.2 Classification of RFID System

RFID systems are often classified as passive (deriving power in the tag from rectifying the incident RF power) or active (battery embedded in the tag and active transmitter) or semi-passive (on-tag power source but no on-tag transmitter). Depending on the programmability, RFID systems can be classified into class0 to class 5. Class 0 is read-only tag, which has an identification code recorded at the time of manufacture, or when attached to certain objects. All the others are read-write tags

which offer additional functionality since they can be written once or many times throughout their life. To be more specific, class 1 is read, write once; class 2 is read, multiple write; class 3 has class 2 capabilities plus a power source; class 4 has class 3 capabilities plus active communication; while class 5 has class 4 capabilities plus the ability to communicate with passive tags.

Passive tags that operate at frequencies up to 100 MHz are usually powered by magnetic induction. An alternating current in the reader coil induces a current in the tag's antenna coil, allowing charge to be stored in a capacitor, which then can be used to power the tag's electronics. Information in the tag is sent back to the reader by loading the tag's coil in a changing pattern over time, which affects the current being drawn by the reader coil — a process called load modulation. Unlike a transformer, the coils of a reader and a tag are separated in space, and coupling between the coils can occur only where the magnetic field lines of the reader coil intersect with the tag coil, i.e., in the near field region. Beyond this distance the energy breaks away from the antenna as propagating waves; this is known as the far field region. The boundary of the near field and far field is governed by the frequency of the alternating current and is approximately limited to a distance of $\lambda/2\pi$. For example, at 13.56 MHz used by the ISO 15693 and 14443 standards, this distance is 3.52 meters, but at 915 MHz, used by EPCglobal, the range of operation if based on near field coupling would be limited to six centimeters, reducing its usefulness. Besides the intrinsic short communication distance, another drawback is that the near field will decay rapidly [1]; proportional to a $1/d^3$ factor, where d is the

distance from the center of the reader coil to the tag. As a result, typical systems operating at 13.56MHz can only achieve a communication distance in the order of tens of centimeters, which is considerably shorter than the near field limit.

To circumvent the range problem at higher frequencies, a different principle is used for RFID systems operating at UHF, namely, propagation of electromagnetic waves in far field region to power the tag. In terms of regulation environment, EPCglobal class-1 Gen2 and ISO 18000 family with the -6 group of documents are dedicated to UHF operation. Typical operation distance is less than ten meters. Fig. 1.3 illustrates the RFID system operation at UHF.

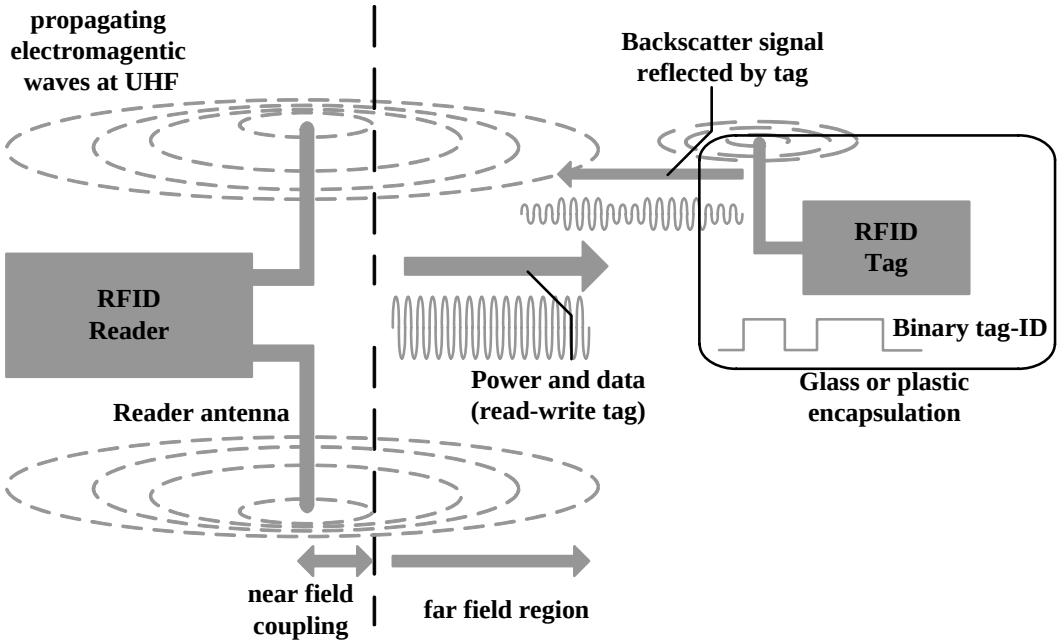


Fig. 1.3 RFID tag operation at UHF

At present, most of interests for RFID implementation are in the UHF band, which offers opportunity to optimize between antenna size and path loss for long-distance applications. The antenna size is of concern because it is a constraining factor of tag's size. At the very minimum, tags should be smaller than the tagged objects. On

the other hand, performance of the system in particular the range is highly dependent on size and shape of antennas, but antenna size is largely dependent on operating frequency. For example, at 5.8GHz, an optimal antenna length is 2.5cm while at 915MHz, it is 16cm. Table 1.1 summaries the features of RFID systems operating at different frequency bands.

Table 1.1 RFID systems at different frequencies and their features

Frequency Ranges	LF 125 KHz	HF 13.56MHz	UHF 860-960MHz	Microwave 2.45GHz&5.8GHz
Typical Max Read Range(passive tags)	Shortest 2.5-30cm	short 5-60cm	Longest ~ 2 to 7m	Medium ~ 1m
Tag power source	Generally passive tags only, using inductive coupling	Generally passive tags only, using inductive or capacitive coupling	Active tags with integral battery or passive tags using capacitive storage or far-field coupling	Active tags with integral battery or passive tags using capacitive storage or far-field coupling
Data Rate	Slower	Moderate	Fast	Faster
Ability to read near metal or wet surface	Better	Moderate	Poor	Worse

1.1.3 Regulation and Standardization

There is no global public body that governs the frequencies used for RFID. In principle, every country can set its own rules. However, of the large amount and variety of RFID applications, object tracking in global supply chains constitutes a large potential markets. Tags must be able to operate between different countries as goods flow globally. For this to happen worldwide readers and tags must be

compatible and common frequency bands should be allocated. Low-frequency (LF: 125-134.2 kHz and 140-148.5 kHz) and high-frequency (HF: 13.56MHz) RFID tags can be used globally without a license. Ultra high frequency band, however, cannot be used globally as there is no single global standard. In the United States, the FCC provides unlicensed spectrum in 902-928MHz band, as governed by part 15, section 247 regulations. When utilizing the FHSS, transmitting power can be 4W EIRP with a channel bandwidth of 500 kHz. In Europe, European Telecommunications Standards Institute (ETSI) EN 302 208-1 v1.1.1 opens the spectrum from 865 MHz to 868 MHz with a channel spacing of 200 kHz and maximum power of 2W ERP. In South Africa, when operating frequency band is 869.4-869.65 MHz, maximum transmitting power is 500mW ERP, when it is 915.2-915.4 MHz, transmitting power can be up to 8W ERP with a channel bandwidth smaller than 250 kHz. In Asia, 952-954 MHz frequency band is allowed for RFID system in Japan, while 908.55-913.95 MHz band is open in Korea with an output power of 4W EIRP. In China, frequency spectrum available for RFID is still under investigation. In New Zealand, spectrum of 864-868MHz is allocated for RFID system operation with an EIRP of 4W; while in Australia 918-926MHz is open with an EIRP of 1W.

There are also various standards regarding RFID technology. Some important ones are listed:

a) ISO 14443: It is a HF (13.56MHz) standard, which is being used as the basis of RFID-based passports under international civil aviation organization (ICAO) 9303.

b) ISO 15693: It is another HF (13.56MHz) standard, which is being used for non-contact smart payment and credit cards.

c) ISO 18000: The 18000 series of standards span most of the frequency bands used in RFID. 18000-2 is for 125 kHz, 18000-3 is at 13.56MHz, 18000-4 at 2.45GHz, 18000-6 for UHF band, 18000-7 for active tags used in asset monitoring and location. Unfortunately, these standards are not completely harmonized or interoperable: for example, ISO18000-6A, B, C use different modulation, packet structures and command sets.

d) EPC Gen2 is short for EPCglobal UHF class 1 Generation 2. This protocol was approved in December 2004, which is aimed to address the problems that had been experienced with Class 0 and Class 1 tags. EPC Gen2 standard is likely to form the backbone of RFID standards moving forward. In 2006, it was adopted with minor modifications as ISO 18000-6C.

Given the babel of prevalent protocols in the RFID world, the object of this project is to build a fully integrated CMOS single-chip RFID reader for UHF passive RFID system, which supports multiple standards with multiple data rates and multiple modulation formats in different electromagnetic environments by a flexible system architecture.

1.1.4 RFID System Fundamentals

As discussed in section 1.1.2, in the near field, fields are reactive and quasi-static, while in the far field they constitute radiating waves. The transition point between the near field and the far field is $\lambda/2\pi$, which is about 0.053m at 900MHz. Therefore

UHF RFID systems operating in the far field achieve coupling through the propagation of electromagnetic waves.

We first discuss the terminologies to describe the radiation properties of an antenna. The electromagnetic field that an antenna radiates varies with antenna type and output power. Certain antennas will be able to concentrate their fields into a narrow beam. Directivity is used to describe how an antenna concentrates its energy in one direction as compared to all the other directions. It is solely determined by the antenna's radiation pattern. Gain of an antenna is defined as 4π times the ratio of radiation intensity in a given direction to the net power input to the antenna.

$$G(\theta,\phi) = \frac{4\pi U(\theta,\phi)}{P_{in}} \tag{1-1}$$

Typically, antenna gain is described relative to an isotropic radiator that radiates energy in all directions uniformly. An isotropic radiator has a gain of 0dB, while a half-wave dipole antenna has a gain of 2.15dB. When describing the gain relative to an isotropic antenna, we denote this by units of dBi. When describing the gain relative to a half-wave dipole antenna, we use units of dBd. As a result, the following relationship holds

$$G[dB] = G[dBi] = G_d[dBd] + 2.15 \tag{1-2}$$

Effective (or equivalent) isotropically radiated power, *EIRP*, is defined as the net input power to an antenna multiplied by its gain relative to an isotropic antenna

$$EIRP = G_t P_t \tag{1-3}$$

Effective (or equivalent) radiated power, *ERP*, is defined as the net input power to an antenna multiplied by its gain relative to a half-wave dipole antenna

$$ERP = G_{td} P_t \tag{1-4}$$

It is obvious that *EIRP* and *ERP* are related by

$$EIRP = ERP \times 1.64 \tag{1-5}$$

Let's consider a transmitter that sends power P_t through an antenna whose gain is G_t. The power density S at a distance of R can be calculated as

$$S = \frac{G_t P_t}{4\pi R^2} = \frac{EIRP}{4\pi R^2} \tag{1-6}$$

It is useful to define an effective aperture A_e, which is based on the antenna's own gain. It essentially can be thought of as a power capture area

$$A_e(\theta, \phi) = \frac{\lambda^2}{4\pi} G(\theta, \phi) \tag{1-7}$$

When simply denoted as A_e without the dependence on angle, it represents the maximum effective area. Simply multiplying the effective aperture by the power density should give the power received by the receiving antenna. Therefore, power received by the tag is

$$P_{tag} = EIRP \times G_{tag} (\frac{\lambda}{4\pi R})^2 \tag{1-8}$$

where G_{tag} is the tag antenna gain.

In a well designed RFID system, communication distance is limited by tag received power rather than reader sensitivity. For example, assume a 4W *EIRP* at frequency of 915MHz, tag requires at least 50μW and G_{tag}=2dB, the maximum distance is calculated to be 9.3m.

After the power is detected by the tag, its response will be sent back to the reader by intentionally varying the load impedance and causing a mismatch in impedance between tag's antenna and load. Some power is to be reflected back through the

antenna and scattered. This is called backscatter modulation. When an electromagnetic wave impinges on irregularities in a medium, the wave may be random dispersed. This phenomenon is called scattering. A useful representation of an object's monostatic scattering characteristics is its backscattering cross section or radar cross section (RCS). RCS is defined as a measure of power scattered in a given direction.

$$\sigma = \lim_{R\to\infty} 4\pi R^2 \frac{\left|E^{scat}\right|^2}{\left|E^{inc}\right|^2} = 4\pi R^2 \frac{P_s}{P_i} \tag{1-9}$$

Where E^{scat} is the scattered electric field, E^{inc} is the incident electric field, R is the distance from the target, P_s is the scattered power and P_i is the incident power.

Therefore, the reflected power from tag P_{refle} is

$$P_{refle} = EIRP \times \sigma \times \frac{1}{4\pi R^2} \tag{1-10}$$

The reader received power P_{rec} can be calculated as

$$P_{rec} = P_{refle} \times G_{reader} \times \left(\frac{\lambda}{4\pi R}\right)^2 = EIRP \times \sigma \times G_{reader} \frac{\lambda^2}{(4\pi)^3 R^4} \tag{1-11}$$

Assume G_{tag}=G_{reader}=0dB, RCS=10cm^2, and keep a 48μW incident power for tag's proper operation. Table 1.2 summaries the calculated communication distance and reader received signal strength.

Table 1.2 link budget calculation at a carrier frequency of 915MHz

Reader Transmit Power(W/dBm)	Tag received power (μW/dBm)	Tag reflected power (μW/dBm)	Communication distance(m)	Reader received power(dBm)
0.0004/-4	48.5/-13.2	5.66/-22.4	0.075	-31.6

0.004/6	47.3/-13.2	5.53/-22.8	0.24	-41.8
0.01/10	47.2/-13.2	5.51/-22.8	0.38	-44.6
0.1/20	47.3/-13.2	5.53/-22.8	1.2	-55.8
0.5/27	46.7/-13.2	5.46/-22.8	2.7	-63
1/30	47.2/-13.2	5.5/-22.8	3.8	-66
4/36	48.5/-13.2	5.66/-22.8	7.5	-71.6

As can be seen from table 1.2, to enhance the communication distance, increase of the transmitting power and reduction of tag power consumption are crucial. It is also preferable for tag antenna to have gain, for example, if G_{tag} is 3dB, reader transmit power is 4W, keep everything else the same, the communication distance can be increased to 10.5m as opposed to 7.5m. Notice that the reader received power is in a comfortable range for detection, therefore the communication distance of a UHF RFID system is normally dominated by the tag power consumption instead of reader sensitivity.

1.2 Brief Introduction to RFID Tag

Although the focus of this work is reader transceiver, it is necessary to understand the basic architecture, challenges and limitations of the tags because the ultimate design goal is to achieve better communication with tags.

Due to the different working principles, tags working at HF and UHF have quite different architecture and circuit implementation. Depending on the protocol, the memory cell on the tag needs to be programmed once or multiple times. In addition, complex functions, such as anti-collision and authentication, are indispensable in the tag in spite of the fact that they need additional operation power. Passive tags, due to their low cost potential, attract much attention nowadays. There have been a lot of passive LF and HF tags reported [2]-[4]. Recent interest has moved to UHF passive

tags. A passive UHF RFID tag IC with only 16.7μW minimum RF input power is reported in [5]. Another passive RFID tags with 36.6% efficiency full wave CMOS rectifier and current-mode demodulator is proposed in 0.35μm FeRAM technology [6]. An RFID tag operating at 2.45GHz is demonstrated in silicon-on-insulator (SOI)-based CMOS technology, which only occupies chip area of $0.15\times0.15mm^2$ [7]. The general block diagram of an UHF RFID tag is shown in Fig. 1.4. The antenna is the only external component of the tag. It provides low loss and is power matched to the average input impedance of the rectifier. The rectifier converts a part of the incoming RF signal power to DC for power supply for all the active circuits on chip. A charge pump converts the dc supply voltage to several high voltages for reading and programming of memory cell. The demodulator converts the input RF signal to digital data and passes it to the digital controller for data processing. The modulator is realized using a backscatter approach. By converting data from the control logic to changes in the input impedance, the electromagnetic wave backscattered by the antenna is modulated. The clock generator can be injection-locked to the input or stand-alone oscillator which provides clocks for digital baseband operations. The logic circuitry handles the protocol, including anti-collision features, cyclic redundancy checks (CRC), etc.

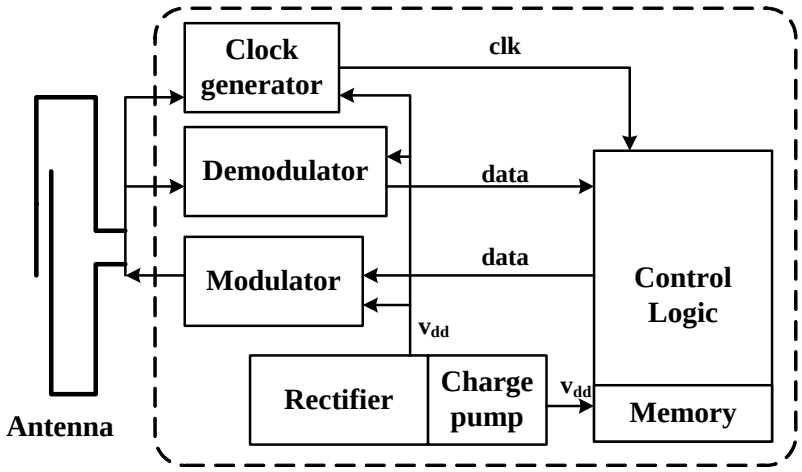


Fig. 1.4 System Architecture of a passive UHF RFID tag

As discussed in section 1.1.4, for longer communication distance, the power efficiency of voltage generator of the tag needs to be maximized, while the circuit power consumption needs to be minimized. Memory cell which is used to store various information such as product ID, manufacturer's ID, etc. is also expected to consume minimum amount of power, require no additional mask and provide reliable performance. Such memory cell with low cost and small area allows more user-programmable memory to be added into a tag, which opens up many new possibilities. From the cost perspective, the total chip area needs to be minimized which prohibits the use of large on-chip capacitors. In addition, all the devices should be standard, CMOS compatible. Besides the basic functionality, i.e. returning a simple identification number, it is future trend to extent advanced features to tags for greater utility. For example, adding a physical sensor to a tag has been an important development, which provides the capability for a storeowner to learn something about the conditions a product has experienced in the past. By incorporating a temperature-sensitive material into the tag, and electronics that can detect a change in

its state (e.g., its electrical resistance might permanently increase), it is possible to determine whether the food could be contaminated.

New applications are being continuously opened up. However, given various constraints, the integration of high performance, low cost, passive RFID tags, perhaps with advanced features remains a very challenging task.

1.3 Issues to be Solved and Future Directions in RFID System

1.3.1 Challenges in RFID Implementation

Although it is believed that RFID is a promising technology which would even significantly change the way people live. Several remaining technical issues for RFID implementation still present a challenge: tag orientation, reader coordination, multiple standards, etc.

a) Orientation of Tag

RFID does not require direct line-of-sight to operate, but the reader cannot communicate effectively with a tag that is oriented perpendicular to the reader antenna. The reception can be improved dramatically by rotating their relative orientation. Imagine when a number of products are placed in a random orientation inside a shopping basket, it become inevitable that some will be invisible to the reader.

Since the tagged product cannot be re-oriented, the solution to this problem is to vary the position of the reader or build advanced antennas that are less sensitive to orientation. One approach is to use many readers that have a diversity of orientations relative to the read area and to sequence through them performing multiple scans

from different directions. The read results are then merged, providing a much greater chance of identifying all of the tags. Another solution employs antenna diversity by using a single reader with several switchable antennas that can be sequentially connected to the reader. This is likely to be a more cost-effective solution because it would reduce the number of components needed to build the system.

b) Dense-Reader Environment

As tags become more common, readers will be deployed on a larger scale, effectively garbling the data for systems in proximity to each other. This problem will become particularly serious if many mobile hand-readers are in use within close range of each other. EPC Gen2 standard aims to address the air interface compliance and performance issues in the dense-reader environment to facilitate and simplify global supply chain visibility.

It is possible that by intelligently filtering out noise when interpreting the tag's signal received at the reader, performance of the system can be improved significantly. However, nearby interference with large amplitude would require high-Q filter which is difficult to achieve. Application of advanced data-coding techniques in the tag may also improve noise immunity and allow some multi-tag signal collisions to be separated and interpreted correctly. However, this may require more costly signal processing in the reader.

c) Multi-Protocol Reader

As noted earlier, several frequencies and standards have been used for RFID system application. In an ideal world, industry would adopt one universal standard; however,

there are cost trade-offs, national frequency use restrictions, politics, etc. A solution to this problem is to build readers that can operate with multiple standards, which can automatically search for tags across a number of frequency bands using a suite of protocols, and be reconfigurable, allowing them to adjust to national frequency restrictions.

d) Product Packaging Independence

Bar codes can be printed on a label and still be readable independent of the contents of the product or packaging. RFID, on the other hand, can be disrupted by materials in the product itself. Because tags use tuned RF circuits to receive interrogation signals, it is possible to detune or attenuate the signals if the tag is placed next to certain types of packaging, for example, ferrous metals and cans. This problem is a challenging one, as the most obvious solution is to change the packaging material, but clearly some products do not have economic alternatives to metal, or metallized packaging, particularly where robustness and airtight storage is required.

1.3.2 Future Directions of RFID Implementation

To facilitate the large-scale adoption of RIFD system, the issues and challenges discussed in 1.3.1 have to be solved first. Meanwhile, people are looking into new applications for RFID system and the way to improve existing systems in terms of read range, cost, etc.

At present, most of the passive UHF RFID systems can read tags at a maximum distance of about a few meters. As the power requirements of the tag reduces and the sensitivity of the reader improves, reliable longer-range systems should become

possible and expand the usefulness of RFID system.

Without doubt, lowering tag and system costs would promote the adoption of RFID, particularly for item-level tagging. Current targets are in the range of 5 US cents or lower at significant volume. Every aspect of the system must be optimized for low cost. Technological innovations become indispensable to reduce the cost of the silicon chip, integrated antenna, the assembly and printing technique.

Privacy is also an issue to be solved. Some privacy groups worry that tags in people's homes might be read by a passing car. Based on the earlier description on the RFID operation principle, now these scenarios are either impossible or very hard to achieve because of the orientation, absorption by building materials, and the limited operation distance. However, if early adopters do not address this issue successfully, they may face customer pushback and loss of sales. As a result, in the EPCglobal Gen2 standard, the "kill" command that can disable a tag at the point of purchase as well as the CRC checking and access password, etc. have been standardized.

Finally, the extensive use of the electronic tagging technology cannot be a success without advanced software systems. Database management software in the future will need to deal with item-level references, track product sales in the event of a recall, respond to data recovered from a tag's writable memory, etc. Many of these processes will need to operate in realtime because tag tracking is automatic and continuous, and the data flow will be derived from products shipped globally across all time zones

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1.4 Organization of This Dissertation

Chapter 2 focuses on the study of system specifications and proposed reader transceiver architecture. System specification is derived based on EPC Gen2 standards and European protocol. After briefly review the transceiver architecture, a suitable architecture for the reader is proposed. Specifications of each building block are derived. In particular, the challenges of the reader are discussed. The effects of the continuous wave are analyzed in detail.

Chapter 3 presents the design and measurement of a fractional-N frequency synthesizer for the reader transceiver. To achieve the target specification, a modified transformer feedback VCO and a 3rd-order single-loop ΣΔ modulator are proposed. The optimization in terms of phase noise and power are performed in the system level of the proposed synthesizer. Detailed design considerations are discussed.

Chapter 4 describes the analog baseband filter and variable gain stage for the reader receiver. It is composed of a tunable active-trap, a continuous time anti-aliasing filter, a variable gain stage and a switched-capacitor channel selection filter. The need and the challenges for a baseband with widely tunable bandwidths are discussed in detail. Design consideration and measurement results are illustrated.

Chapter 5 presents the circuit design and experimental results of the other building blocks in the reader transceiver, including the receiver front-end, A/D converter, transmitter, D/A converter, as well as the reader digital baseband.

Chapter 6 introduces the theoretical study of the reconfigurable baseband. Noise in a sampled system is discussed first. The power in CSF and ADC are optimized subject

to the constraints on noise and settling requirement. Reconfigurablility in terms of the clock frequency, baseband architecture and dynamic range are discussed.

Chapter 7 describes the measurement results of the proposed reader. The consideration for the layout floorplan is discussed. Experimental results about the receiver, receiver with ADC, transmitter and transmitter with DAC are shown. The performance of the proposed reader transceiver is summarized.

Chapter 8 presents the conclusion and potential future improvement of this work.

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Chapter 2
SPECIFICATION, ARCHITECTURE AND FEATURES OF THE PROPOSED RFID READER

2.1 Transceiver Architecture Overview

In today's world of miniaturization, there is an increasing industry pressure to reduce the cost of communication chips. This pressure has driven designers to develop transceivers with higher level of integration. One of the primary goals of this dissertation is to explore techniques for implementing the RFID reader in an inexpensive complementary metal-oxide-semiconductor (CMOS) technology, which now offers higher integration level and processing speed of the baseband DSP circuits. The benefits conveyed by integration are self-evident: minimization of the number of off-chip components (particularly the number of expensive passive filters), low power consumption, improved form factor, reduced cost and ease of design. However, RF circuit design becomes more challenging without the traditional more expensive technologies like GaAs or silicon bipolar which are optimized to provide signal amplification at radio frequencies. In addition, replacing the external components with on-chip components requires a comprehensive overhaul of the front-end design. Therefore, Neoteric transceiver architectures, clever circuit design techniques and mature solid state technology have become the indispensable

premises. To receive and process signals with minimum cost and power, to facilitate the integrated implementation, various receiver topologies have surfaced in recent years, each having advantages and disadvantages.

2.1.1 Receiver Architecture

a) Superheterodyne

Fig. 2.1 shows a typical superheterodyne receiver. The signal is first amplified then translated to a much lower intermediate frequency (IF) anywhere from 10MHz to 100MHz, where it is substantially amplified and filtered by highly-selective passive bandpass filters. The choice of IF is critical in determining the selectivity and the sensitivity of the receiver. Lower IF is favorable in terms of selectivity, but image rejection becomes the bottleneck, and vice versa. Because the Local Oscillator (LO) operates at a different frequency of incoming signal, LO leakage and DC offset problems do not hamper the system performance. As a result, generally this approach is thought to provide high selectivity and sensitivity. However, there is some cost penalty due to the requirement of several high-Q band-pass filters to achieve adequate image rejection and channel selection, which are usually realized as passive and external components. Amplifying signals at IF also increases power consumption because transistors must be biased at large currents to drive the parasitics and the low characteristic impedance of the passive IF filters. All these tradeoffs make it difficult to achieve high level integration on a single chip.

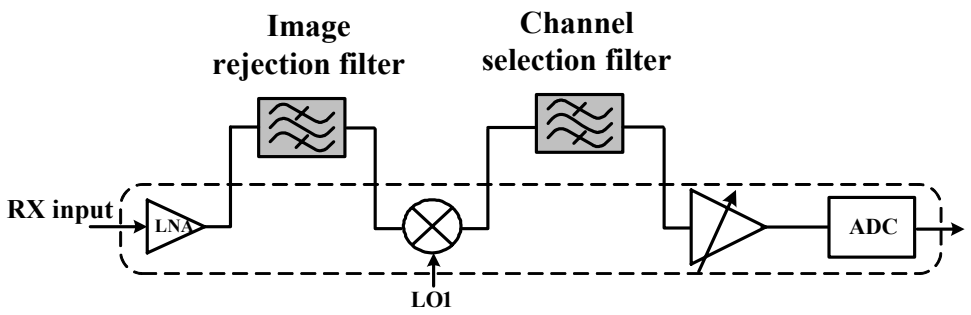


Fig. 2.1 Superheterodyne receiver

b) Single-Conversion Zero-IF

Direct-conversion architecture has been well-recognized for monolithic integration as shown in Fig. 2.2. It is also known as a zero-IF receiver because the LO is centered at the signal carrier frequency and thus the first IF, in the context of a superheterodyne receiver, is zero. RF preselection may in principle be removed because there is no image channel. In practice, it is still required to suppress strong out-of-band signals that may create large intermodulation distortion in the front-end prior to baseband channel selection and to avoid harmonic downconversion. Only a lowpass filter, which is in effect a bandpass filter centered at DC when the negative frequency axis is included, is used to select the desired channel and to reject all adjacent channels. All amplification is performed in baseband, therefore saving area and power. A quadrature down-conversion generates I and Q signals for further signal processing.

Since a zero-IF topology converts the intended band to zero frequency, extraneous offset can corrupt the signal and, more importantly, saturate the following stages. In particular, since LO is of the same frequency as RF, self-mixing caused by LO leakage exacerbates the problem by inducing a time-varying DC offset. DC Offsets

also come from other sources: transistor mismatch in the signal path between mixer I and Q inputs to the detector; or a large undesired near-channel interferer leaking into the LO port of the mixer and self-downconvert to DC. Moreover, flicker noise, which is still not well understood in MOS transistors, substantially corrupts the signal close to zero frequency. The architecture is also more prone to second-order inter-modulation distortion product (IM_2). Nevertheless, the aggregate of single-conversion zero-IF's advantages for a miniature, low power transceiver warrants continued research and development.

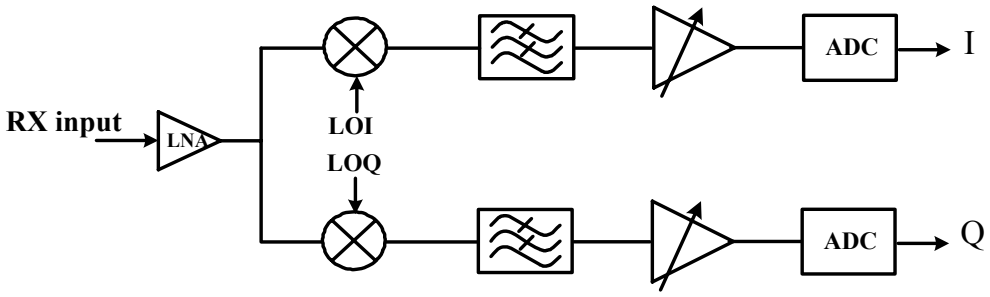


Fig. 2.2 Direct-conversion zero-IF receiver

c) Dual-Conversion Zero-IF

Dual-conversion zero-IF provides an effective way of combining the above discussed superheterodyne and direct-conversion architectures to optimize power consumption and performance. As shown in Fig. 2.3, this approach uses the first IF at high frequency which normally falls out of the application band so that the RF filter following the antenna also acts as an image filter. The desired signal is then down-converted to DC using a complex mixer, so it is equivalently selected by a variable LO_2. This architecture is amenable to integration due to the following facts.

First, by two step down-conversion, the LO_1 is at lower frequency, which eases the design of a low phase noise high frequency synthesizer that leads to reduction in power consumption. Second, the absence of high-Q image rejection filter, baseband channel selection and amplification again reduce the consumed power. Although the LO leakage doesn't exist, this topology is still plagued by DC offset and IM_2 distortion.

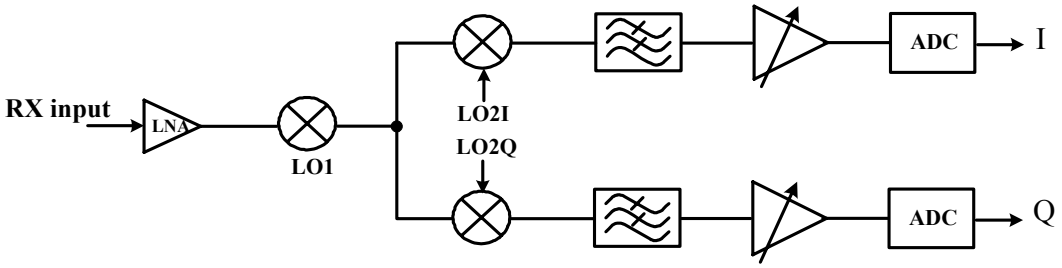


Fig. 2.3 Dual-conversion zero-IF receiver

2.1.2 Transmitter Architecture

A transmitter performs modulation, upconversion, and power amplification. Issues such as noise, interference and band selectivity are usually more relaxed as compared to the receiver, so transmitter architectures are found in only a few forms. However, similar to a receiver, the ultimate goals of a transmitter design are low-power as well as low manufacturing cost. For integrated transceivers, it is cost effective to share the same frequency synthesizer in both the receiver and transmitter, which impose another constraint in the choice of transmitter architecture once that of the receiver is chosen.

a) Direct conversion transmitters

Direct-conversion, also known as homodyne, architecture is favored due to its low power dissipation, and ease of high level of integration. In order to be more spectral

efficient, the transmitted signal in digital communications is usually single-sideband (SSB) with suppressed-carrier output. However, it would demand a high-order RF filter with a sharp transition to sufficiently suppress one sideband and carrier while passing the desired sideband band. An alternative method is to use quadrature upconversion proposed by Weaver in 1956 as shown in Figure 2.4. Depending on whether the outputs of the I and Q branches are added or subtracted, the final output will select either the upper or the lower sideband. Nevertheless, the unwanted sideband is not completely suppressed due to unavoidable gain and phase mismatches between the baseband I and Q branches as well as the two quadrature LO outputs.

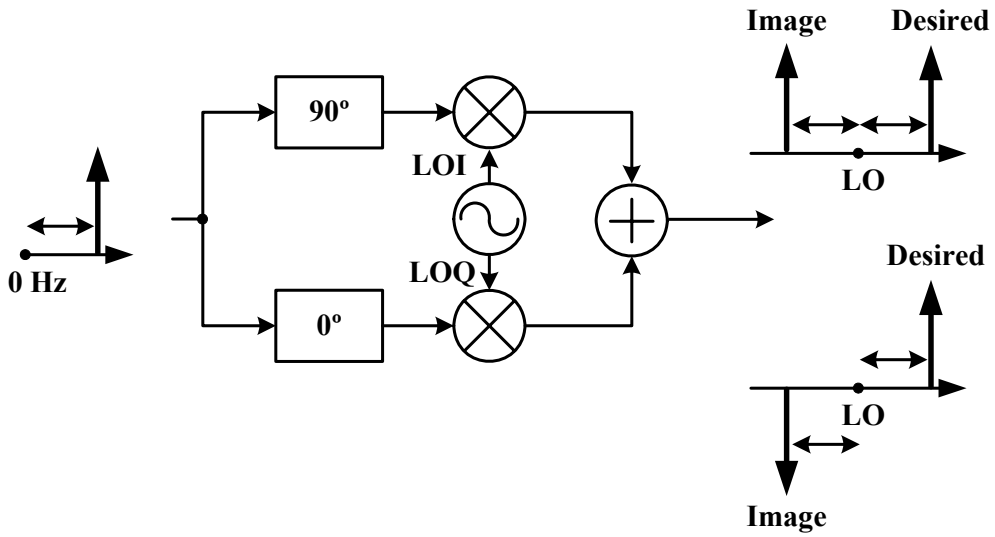


Fig. 2.4 Single-sideband direct upconversion

In a direct conversion transmitter, the transmitted carrier frequency is the same as the LO oscillator frequency as shown in Fig 2.5. This architecture suffers from the disturbance of the local oscillator by the power amplifier, which is called “injection pulling” or “injection locking”. Another drawback is LO leakage as the LO

frequency is centered in the transmission band, which will appear as a transmitted tone at the LO frequency and interfere with the intended transmitted data signal at the receiver's front-end.

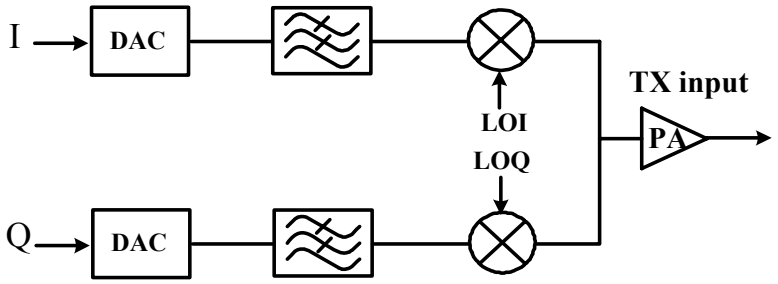


Fig. 2.5 Direct-conversion transmitter

b) Two-Step Transmitters

To circumvent the problem of LO leakage and frequency pulling in the direct-conversion transmitter, the upconversion of baseband signal to RF can be performed in two steps so that the PA output frequency is far from the two LO frequencies as shown in Fig 2.6. Another advantage over the direct conversion approach is that since the quadrature modulation is performed at lower frequencies, better I and Q matching can be achieved.

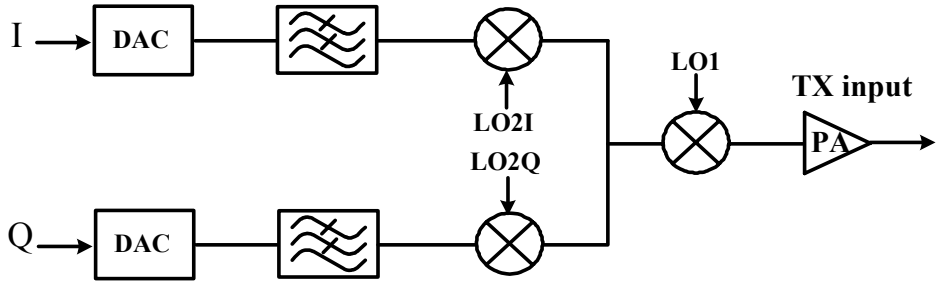


Fig. 2.6 Two-step transmitter

2.2 Transceiver Fundamentals

2.2.1 Sensitivity and NF

One of the key receiver system requirements is sensitivity, which is a measure of its

ability to amplify and demodulate weak signals. Sensitivity is often expressed in terms of the minimum detectable signal (MDS) level at the antenna which provides an adequate signal-to-noise ratio (SNR) at the receiver output for demodulation. MDS is calculated by

$$MDS = -174dBm/Hz + NF + 10\log BW + SNR_{\min} \tag{2-1}$$

where -174 dBm/Hz is the thermal noise at 290°K, *NF* is the accumulative noise figure of receiver in dB, *BW* is the system bandwidth used in SNR calculation of the demodulator, and $SNR_{\min}$ is the minimum signal-to-noise ratio required by the demodulator to maintain a certain level of fidelity, typically represented by bit error rate (BER). The receiver input noise floor is thus

$$Noise\ floor = -174dBm/Hz + 10\log BW \tag{2-2}$$

Noise from the electronics is described by noise factor *F*, which is a measure of how much the signal-to-noise ratio is degraded through the system. Noise factor is typically defined in 1 Hz noise bandwidth and it is called spot noise factor. When noise factor is expressed in decibels, it is called noise figure (NF). *NF* of a circuit block can also be expressed as the amount of *SNR* degradation due to the additional noise, i.e.

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{SNR_{in}}{SNR_{out}} \tag{2-3}$$

$$NF = 10\log_{10} F \tag{2-4}$$

where *S* is signal power, *N* is noise power, subscripts *in* and *out* represent input and output. For an amplifier with input referred noise voltage v_n, and current noise i_n as shown in Fig. 2.7, *NF* can be calculated as [1]

$$NF = 10\log\left(1+\frac{\overline{(v_n + i_n R_s)}^2}{4kTR_s}\right) \tag{2-5}$$

For low frequency CMOS circuit, i_n is approximated to 0. Therefore, (2-5) can be simplified to

$$NF = 10\log\left(1+\frac{\overline{v_n}^2}{4kTR_s}\right) \tag{2-6}$$

It is sometimes useful to represent the building block noise in terms of equivalent noise power v_n^2 (V^2/Hz). From (2-6), we have

$$v_n^2 = 4kTR_s \times (F-1) \tag{2-7}$$

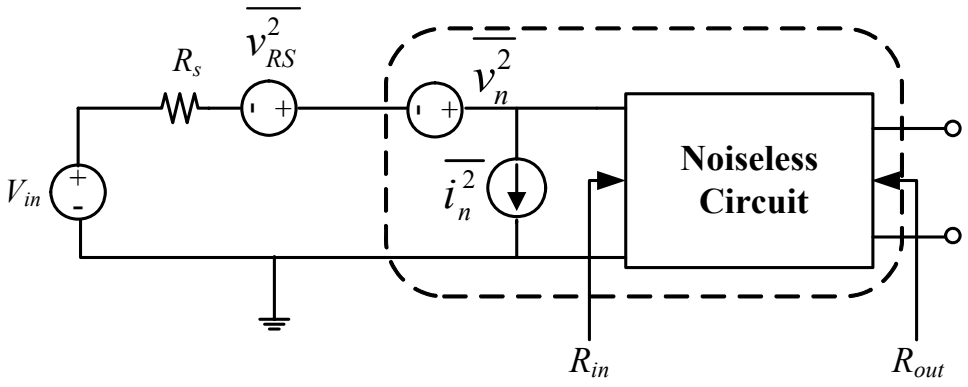


Fig. 2.7 Calculation of noise figure

For components in series, the accumulative noise factor can be calculated as

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{2-8}$$

where F_i is the noise factor of i_{th} stage, G_i is the available power gain of i_{th} stage which is defined as

$$G_i = \left(\frac{R_{in,i}}{R_{out,i-1} + R_{in,i}}\right)^2 A_{vi}^2 \frac{R_{out,i-1}}{R_{out,i}} \tag{2-9}$$

Where $R_{in,i}$ is the input resistance of the i^{th} stage, $R_{out,i}$ is the output resistance of the i^{th} stage, $A_{v,i}$ is the voltage gain of the i^{th} stage.

Formula (2-8) is known as Friis equation. It shows how the noise of later building blocks is suppressed by the presence of preceding gain stage. For this reason, typically a low noise amplifier is placed at the front of a receiver.

2.2.2 Linearity and Distortion

Ideally, the output is expected to be linearly related to the input. In reality, nonlinearity always exists due to active, passive devices in the circuits or the signal swing being limited by the power supply rails.

One of the most common ways to test the linearity of a circuit is to apply two signals at the input, having equal magnitude and offset by some frequency (ω_1 and ω_2). Although 2^{nd}-order terms can be eliminated by balanced architecture, 3^{rd}-order intermodulation (IM3) lies at the frequency of $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ falls in the band of interest and therefore cannot be easily filtered out. These two tones are referred to as third-order intermodulation terms (IM3). In reality, IM3 may be generated by large neighborhood, which lies close to the desired signal.

Plot fundamental output and IM3 as a function of the input power as shown in Fig. 2.8. The third-order intercept point is a theoretical point where the amplitudes of the intermodulation tones at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ are equal to the amplitudes of fundamental tones at ω_2 and ω_1. It can be seen that the third-order intercept point cannot be measured directly, since by the time the amplifier reached this point, it would be heavily overloaded. Therefore, it is useful to describe a quick way to extrapolate IIP3 at a given power level. In the small signal region, at the intercept point, the IM3 terms have a slope of 3 and the fundamental terms have a slope of 1,

so we have

$$\begin{cases} \dfrac{OIP3 - P_1}{IIP3 - P_i} = 1 \\ \dfrac{OIP3 - P_3}{IIP3 - P_i} = 3 \end{cases} \tag{2-10}$$

where P_1 is the output power at fundamental frequency and P_3 is power at the IM3 frequency for a given input power of P_i. Solving (2-10) results in

$$IIP3 = P_i + \frac{1}{2}(P_1 - P_3) \tag{2-11}$$

Similarly, the second order intercept point can be defined. IM2 terms rise at 40dB/dec rather than 60dB/dec, as in the case of IM3 terms.

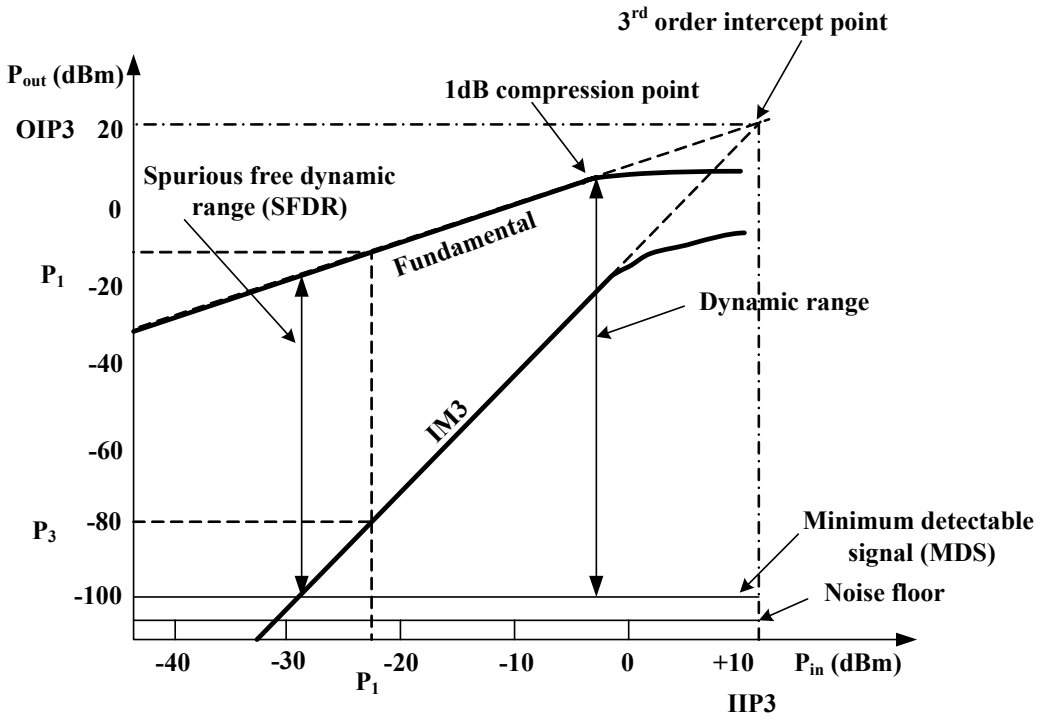


Fig. 2.8 Output power of fundamental and IM3 versus input power

In addition to IIP3 and IIP2, the 1-dB compression point is another common way to measure the linearity. The 1-dB compression point is simply the power level, specified either at the input or output, where the output power is 1dB less than it would have been in an ideally linear device. It is also illustrated in Fig. 2.8. Analysis

reveals that for a single tone, the compression point is about 10dB below the intercept point, while for two tones, the 1-dB compression point is close to 15dB below the intercept point [2].

Finally, for components in series, the accumulative IIP3 can be expressed as

$$\frac{1}{A_{IP3}^2} = \frac{1}{A_{IP3,1}^2} + \frac{A_{v,1}^2}{A_{IP3,2}^2} + \frac{A_{v,1}^2 A_{v,2}^2}{A_{IP3,3}^2} + \cdots \tag{2-12}$$

Where $A_{IP3,i}$ is the IP3 of the ith stage, $A_{v,i}$ is the voltage gain of the ith stage, A_{IP3} is the total IP3.

2.2.3 Dynamic range

So far, we have discussed noise and linearity in the receiver. The former determines the minimum signal that a receiver is able to handle, while the latter determines the maximum signal that a receiver can tolerate. If operation up to the 1-dB compression point is allowed (10% distortion, or IM3 is about -20dB with respect to the fundamental output), the dynamic range is defined as the difference between the output 1-dB compression point and MDS as illustrated in Fig. 2.8.

If we define the upper end of dynamic range as the maximum input level in a two-tone test for which the IM3 products do not exceed the noise floor and the lower end on the MDS, such a definition is called the spurious free dynamic range (SFDR), which is graphically illustrated in Fig. 2.8 and can be express as

$$SFDR = \frac{2(P_{IIP3} - F)}{3} - SNR_{\min} \tag{2-13}$$

where *F=-174dBm+NF+10logBW.*

The SFDR represents the maximum relative level of interferers that a receiver can tolerate while producing an acceptable signal quality from a small input level.

2.3 Specification of the Reader Transceiver

2.3.1 System Overview

Up to now, we have reviewed transceiver architectures and RF fundamentals. Unlike the other communication system, such as GSM, WLAN and UWB, RFID has an asymmetrical up-link and down-link. The ultimate optimization goal is simple tag architecture for low cost passive tags. As a result, RFID system has a distinctive air interface protocol, which results in unique design challenges and features of an RFID reader. In this project the specifications are derived based on the following standards and documents:

a) EPC^{TM} Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocols for Communications at 860MHz – 960MHz Version 1.0.8 [3].

b) ETSI EN 302 208-1 v1.1.1, Electromagnetic compatibility and Radio spectrum Matters (ERM); Radio Frequency Identification Equipment operating in the band 865 MHz to 868MHz with power levels up to 2W [4].

c) FCC rule part 15, section 247 regulations [5].

Some important parameters related to the proposed RFID reader system specification are listed and summarized in table 2.1 and table 2.2.

Table 2.1 Important parameters specified in the EPC class-1 generation-2 protocol that are related to RFID reader design

	Parameter	Description	Subclause	RFID reader parameters
Interrogator to Tag (R => T)	Data Coding	Pulse Interval Encoding	6.3.1.2.3, Figure 6.1	Power spectrum of transmitter
	Modulation	DSB-ASK,	6.3.1.2.2	TX needs SSB

		SSB-ASK, PR-ASK		up-conversion
	Modulation depth	90% nominal	6.3.1.2.5, Figure 6.2, Table 6.6	Modulation depth control
	Bit Rate	26.7kbps to 128kbps	6.3.1.2.4	TX DAC clock frequency
	Transmit mask		Figure 6.6, 6.7	TX linearity
	Frequency accuracy	+/-10ppm	6.3.1.2.1	Frequency synthesizer
Tag to Interrogator (T => R)	Data Coding	Baseband FM0 or Miller-modulated subcarrier (selected by the interrogator)	6.3.1.3.2	1)Power Spectrum Density determines the RX bandwidth 2) BER vs. SNR determines the RX NF
	Modulation	ASK and/or PSK modulation (selected by tag)	6.3.1.3.1	Universal RX structure that can be used for both cases
	Bit Rate	FM0: 40kbps to 640kbps; Subcarrier modulated: 5kbps to 320kbps	6.3.1.3.3 Table 6.11	Receiver BW tuning range

A modern communication system operates in a TDD or FDD fashion to minimize the signal interference between receiver and transmitter, for example, GSM: 935MHz to 960MHz receive and 890MHz to 915MHz transmit. As described in EPC Gen2 standard and shown in Fig. 2.9, in order to provide power to passive tags, an interrogator is required to transmit a continuous wave (CW) when receiving the response from tag. Moreover, the CW and tag's response are at the same frequency since tag replies by backscatteing. The large continuous wave will couple directly from TX to RX as a strong self-interference. Its effects will be analyzed in detail in section 2.5.1. As a result, to allow the simultaneous transmission of TX and RX, dual

antennas for the reader is a favorable choice because it can provide a better isolation (around 40dB at UHF) provided the two antennas are separated far enough, while other approach such as circulator can only have 20dB isolation. To halt the transmission of the CW, one way is to store the energy on the tag. However, this would result in prohibitively large on-chip capacitors, which in turn causes larger chip area and subsequently higher cost.

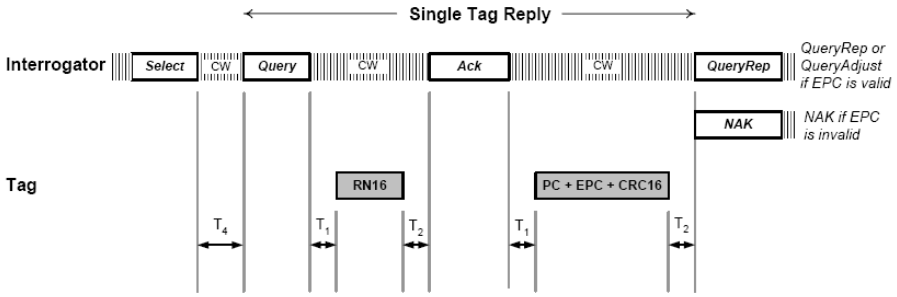


Fig. 2.9 R=>T and T=>R Link timing

Table 2.2 Important parameters specified in the ETSI 302 208-1 specification that are related to RFID reader design

	Parameter name	Description		Subclause	Remark
Interrogator to Tag (R => T)	Frequency accuracy	+/-20ppm		8.1.3	Frequency synthesizer
	Radiated power (ERP)	865M-868M	20dBm	8.3.3	Transmit power
		865.6M-868M	27dBm		
		865.6M-867.6M	33dBm		
	Transmit mask			8.4.3	Transmitter ACPR
Tag to Interrogator (T => R)	Receiver threshold in *listen* mode	Transmit power	Threshold (ERP)	9.1.3 Table 6	Receiver sensitivity
		Up to 100mW	≤-83dBm		
		101mW to 500mW	≤-90dBm		
		501mW to 2W	≤-96dBm		
	Blocking or desensitization in *listen* mode			9.3.3	Receiver selectivity and

	Adjacent sub-band selectivity in *talk* mode		9.4.3	linearity, frequency synthesizer phase noise
	Blocking or desensitization in *talk* mode		9.5.3	

As can be seen in table 2.2, there are two distinct operation modes: listen mode and talk mode. Prior to each transmission by a reader, its receiver shall switch to the listen mode and monitor a selected sub-band. Any signal detected by the receiver in excess of the threshold level shall indicate that another equipment already occupies the sub-band. Only when a vacant band is detected, the reader is allowed to switch to talk mode. In consequence, in the listen mode, the reader only receives without transmits, i.e., the high power CW to power the passive tag doesn't exist. While in the talk mode, the reader is ready to communicate to tags, so it has to transmit the CW during each interrogation round as depicted in Fig. 2.9. In conclusion, the unique operation necessitates different requirements of the reader in each mode.

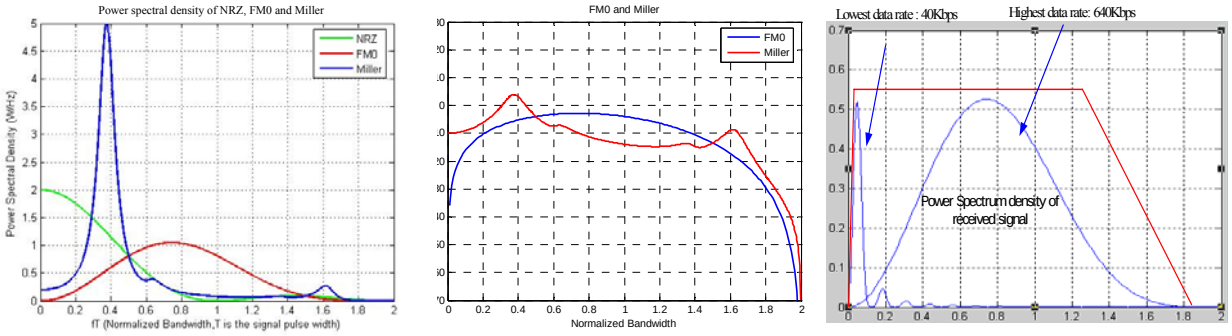
In the United States, the FCC provides unlicensed spectrum in the 902–928 MHz band, as governed by Part 15, Section 247 regulations. These rules permit radiated power up to 1W total, 4W effective isotropic radiated power (EIRP). Spread spectrum techniques are required, either direct sequence or frequency hopping, with channel separation of 25 kHz and out-of-channel emissions 20 dB down in the latter case. If the 20dB bandwidth of the hopping channel is 250 kHz or greater, the system shall use at least 25 hopping frequencies and the average time of occupancy on any frequency shall not be greater than 0.4 seconds within a 10 second period. The maximum allowed 20dB bandwidth of the hopping channel is 500 kHz. As stated

above, the hopping speed is quite slow, which implies a relaxed switching time requirement of the frequency synthesizer.

Note that all the regulations about transmitter power and bandwidth only apply to the reader transmitter, but not the backscatter emissions of passive tags. The US regulations (FCC) qualify a passive radiator as an "unintentional" radiator as they have investigated the emissions in general to be so trivial. The US/FCC maintains the position of not requiring any tests of emissions with RFID tags as it is not relevant.

2.3.2 Receiver Bandwidth, NF and IIP3

The receiver BW is determined by the data rate, coding and modulation scheme adopted of the tag to reader communication link in EPC Gen2 specification (table 2.1). Power spectrum density (PSD) of FM0 and miller coding has a DC-free characteristic as illustrated in Fig. 2.10 [6]. The BW is about twice the Link Frequency (LF). Therefore, for a LF of 40kbps to 640kbps, the receiver bandwidth is calculated to be 80 kHz to 1.28 MHz, while the high-pass corner is about 0.3 times the bit rate, i.e., 12 kHz to 192 kHz.



(a) (b) (c)

Fig. 2.10 Power spectrum density (a) NRZ, FM0 and Miller; (b) FM0 and Miller in dB scale; (c) FM0 (highest and lowest data rate)

According to ETSI 302 208-1, the target listen mode sensitivity is -90dBm for an output power of 101mW to 500mW, while in talk mode the sensitivity of the receiver is determined by the provider in accordance with the needs of the application, so it is not explicitly stipulated in the regulation. As such, the specification is derived based on the listen mode sensitivity, which is much lower than talk mode sensitivity as will be discussed in section 2.5.1.

The modulation from tag to reader may be ASK or PSK. Depicted in Fig. 2.11, the reader baseband algorithms achieves BER of 10^{-3} at SNR of about 10.5dB for FM0 with ASK modulation and 8.5dB for worst case Miller subcarrier (M=2) with ASK modulation. For PSK modulation scheme, the SNR is another 3dB lower than ASK. Thus, the NF is calculated for listen mode sensitivity of -90dBm and SNR of 11dB according to (2-1) and summarized in table 2.3.

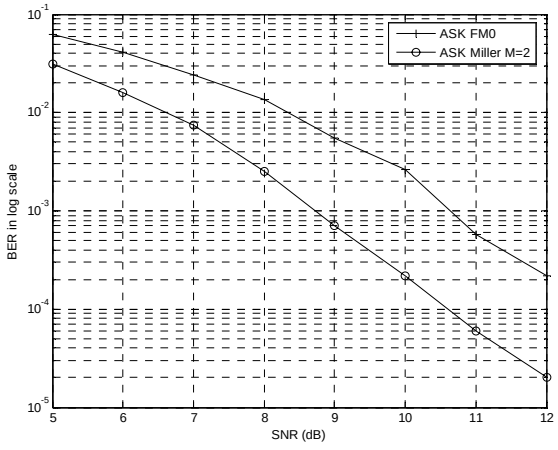


Fig. 2.11 Simulated BER versus SNR for ASK/FM0 data

Table 2.3 NF for sensitivity (-90dBm) and SNR_{out} (11dB) at different BW

Tag to Reader data rate (kbps)	40	80	160	320	640
RX bandwidth (kHz)	80	160	320	640	1280
NF (dB)	24	21	18	15	12

The IIP3 specification calculation is based on the blocking profile. Fig. 2.12 shows

the graphical representation of the blocking profile specified in ETSI 302 208-1 for talk mode and listen mode respectively [4].

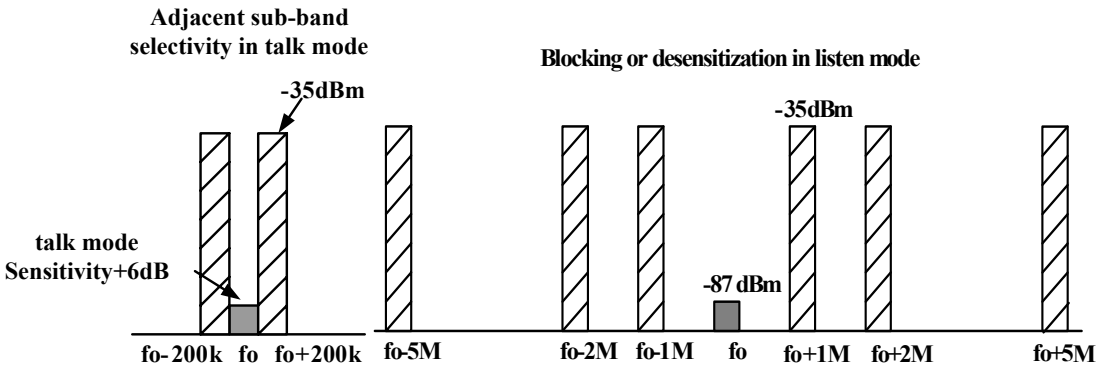


Fig. 2.12 Blocking profile in ETSI 302 208-1

The worst case talk mode blocker is the adjacent sub-band which is -35dBm located at 200 kHz away. The worst case listen mode blockers have a power of -35dBm at 1MHz, 2MHz, 5MHz and 10MHz. However, it make more sense to assume the two interference tones are always at adjacent and alternate adjacent channels whose spacing is the channel bandwidth, instead of two fixed frequency offset, because our targeted multi-protocol reader has a variable data rate and RX bandwidth. The IIP3 is calculated as shown in Fig. 2.13 [7]. Assume two input tones with the same magnitude of -35dBm. Their intermodulation product should be no larger than input referred noise floor of -98dBm, so for a given desired signal of -87dBm and SNR_{out} of 11dB, IIP3=-35+(101-35)/2=-2 dBm.

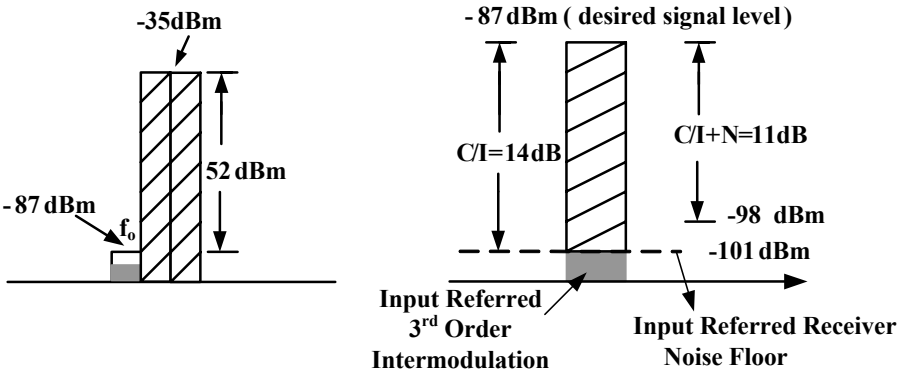


Fig. 2.13 IIP3 calculation

2.3.3 Baseband Filter and ADC Dynamic Range

After the RF signal is down-converted to baseband, the signal is still very weak but interference can be significantly stronger. This results in a large dynamic range of baseband stages. There are typically three kinds of baseband channel selection, analog, digital and mixed-mode [8] as illustrated in Fig. 2.14-2.16. Their pros and cons are summarized and compared in table 2.4.

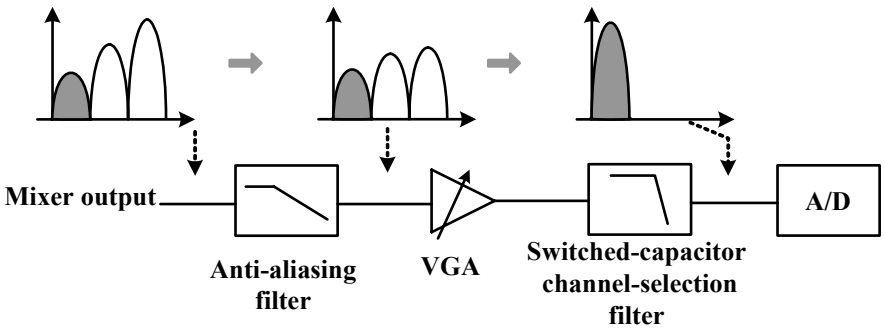


Fig. 2.14 Analog channel selection with a switched-capacitor (SC) filter

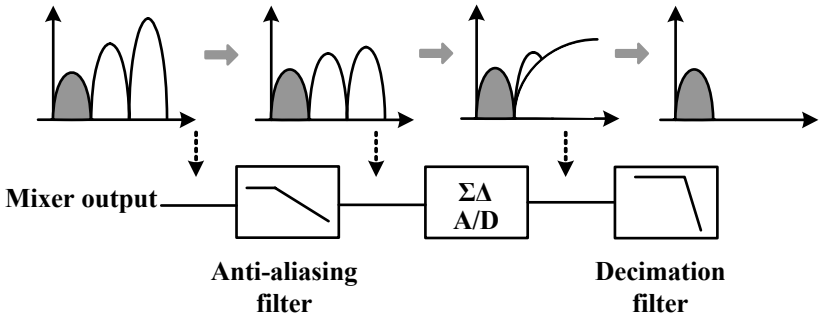


Fig. 2.15 Digital channel selection with a switched-capacitor ΣΔ A/D converter

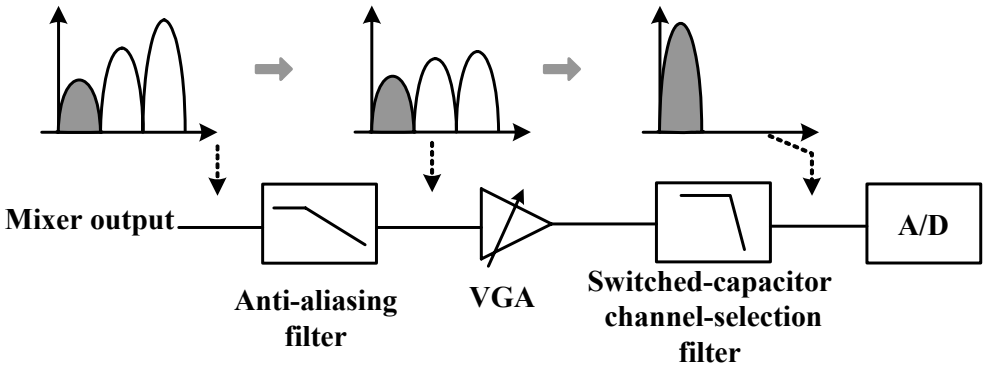


Fig. 2.16 Mixed-mode channel selection with a SC filter and ΣΔ A/D converter

Table 2.4 Features, pros and cons, suitable system applications of the three baseband architectures

	Analog	Digital	Mixed-mode
Filtering	Analog domain filtering prior to A/D	Digital decimation filtering	Both analog and digital domain filtering
A/D requirement	Nyquist A/D, Lower resolution	Over-sampling A/D Highest resolution	Over-sampling A/D Modest resolution
AGC control	1) Only desired signal present to ADC, dynamic range set by the input power variation; 2) AGC needed to amplify the signal to a specific level	1) Large interferers present which set the largest input power to ADC; 2) AGC cannot improve dynamic range	Both desired signal and interferers present at ADC input
Challenges	Fast roll-off; large dynamic range analog channel-selection filter	Large dynamic range ΣΔ A/D converter: either large over-sampling ratio or high order	Relaxed requirement of both channel-selection filter and ΣΔ A/D converter
Cons	Power hungry channel-selection filter	Requires a digital decimation filter at high clk frequency	Both analog channel-selection filter and digital decimation filter are needed
Pros	High speed	1) Better programmability 2) Small overall gain in analog	May be most power efficient

		part	
Suitable application	Wide band systems with small dynamic range e.g.: WLAN, UWB	Narrow band systems with large dynamic range e.g.: GSM	

The dynamic range of the system is determined on the high-end by the maximum signal level presented at the ADC input and on the low-end by the allowable input noise contribution from the ADC to the overall receiver noise figure [7]. As shown in Fig. 2.17, assume no analog filter before ADC (digital channel selection), i.e., largest dynamic range of ADC, system calculation shows that required ADC dynamic range for RFID receiver is around 71dB. In this work, to develop a multi-protocol RFID system that features a system bandwidth in the order of 1MHz and dynamic range of about 70dB, it is preferable to adopt digital or mixed-mode channel selection.

There is a trade-off between the baseband filtering and ADC dynamic range. A higher order filter leads to a low-resolution ADC while a lower order filter must be combined with a high-resolution (large dynamic range) ADC to cope with the signal and large blockers. Following the analysis in [9], for a desired signal of -90dBm and highest blocker of -35dBm, assume the ADC quantization noise is 15dB lower than the desired signal, the ADC's DR is calculated as: -35-(-90)+15=70dB, which yields a similar number with the system calculation results shown in Fig. 2.17. If mixed-mode channel selection is adopted, assume the channel selection filter has 35dB attenuation on the adjacent channel and SNR_{out} is 11dB, ADC quantization noise is 20dB below the thermal noise floor, the ADC's DR is: -35-35-(-90)+11+20=51dB.

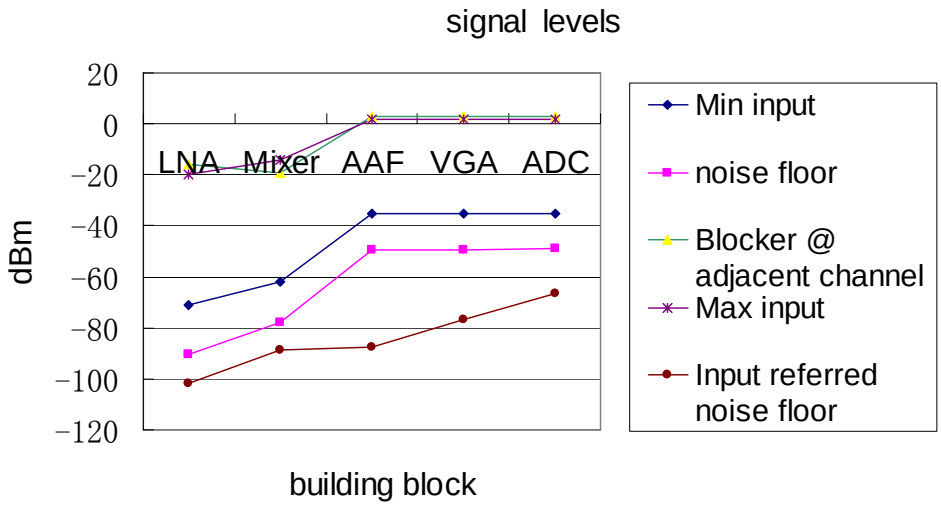


Fig. 2.17 ADC dynamic range in the proposed RFID receiver

However, it is still not clear which one will outperform in terms of power consumption and performance, digital selection or mixed-mode selection, as it will highly depend on the real circuit implementation, especially when a digital decimation filter is involved which complicates the analysis. As a result, both architectures are implemented in the proposed baseband so that it is able to be reconfigured to be either one. Detailed analysis of various tradeoffs and proposed reconfigurable baseband are presented in chapter 6.

Table 2.5 Specifications of channel-selection filter and ADC for both options at the maximum system bandwidth of 1.28MHz.

Channel selection	Channel selection filter attenuation (dB)	Channel selection filter f_{clk} (MHz)	ADC dynamic range (dB)	ADC f_{clk} (MHz)	Oversampling Ratio (OSR)
Digital	N/A	N/A	71	61.44	24
Mixed-mode	35	40.96	51	40.96	16

Now we can calculate the maximum gain of the receiver chain, which has to be decided by the blocking signal since neither digital nor mixed-mode completely filters out the interference. Due to the lack of filtering, when the signal is small and

interference is strong, the largest signal present at ADC input is not the intended signal but the interference and gain is relatively low since the interference amplitude is large; when the signal is larger than the interference, we need to lower the receiver gain to avoid saturation. For digital channel selection, the largest adjacent channel blocker is -35dBm, the optimal input level for ADC is about $0.6V_{peak}$ differential, which is 5.5dBm at 50Ω, assume the baseband stage (trap and AAF) before ADC has adjacent channel attenuation of 15dB, thus maximum gain is calculated to be: 5.5-(-35)+15=55.5dB. Similarly, For the mixed-mode channel selection, assume the entire baseband has adjacent channel attenuation of 35dB, the maximum gain is: 5.5-(-35)+35=75.5dB. While in the analog channel selection approach, the interferences are completely filtered, the maximum gain is: 5.5-(-90)=95.5dB. To leave more design margins, the peak gain is designed to be 95.5dB.

2.3.4 Transmitter Linearity and Output Power

Assume the reader antenna gain is 6dBi, to get 4W EIRP (36dBm), the output power of transmitter is 30dBm. It is difficult for CMOS on-chip power amplifier to generate large power as 30dBm with satisfactory efficiency; hence an external PA is adopted while the RF variable gain pre-amplifier is fully integrated on-chip with an output power of around 8dBm and 20dB gain control range.

The spectrum mask shown in Fig. 2.16 is specified in EPC Gen2 standard. Tari can take the value of 6.25μs, 12.5μs and 25μs. Due to the absence of complete baseband modeling of the PIE encoded ASK data, it is difficult to generate well band-limited baseband transmitting data using verilog-A model or in ADS. As a result, accurate

behavior simulation cannot be accomplished. Calculation is carried out to estimate the transmitter linearity requirement. The OIP3 is calculated to be 8+30/2=23dBm, based on the ACPR of 30dB and output power of 8dBm. Several dB design margins are required since the actual modulated output is more complicated than a single tone.

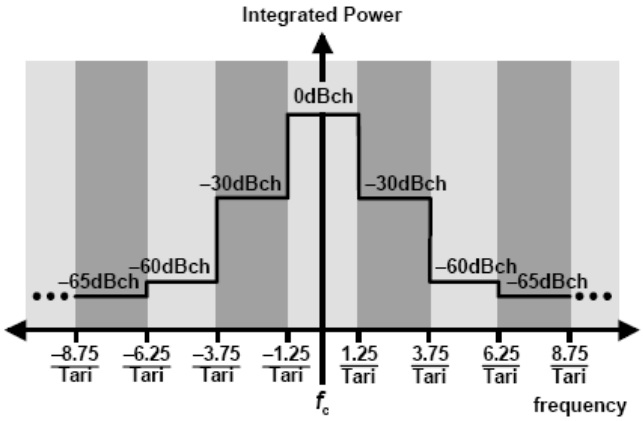


Fig. 2.18 Transmit mask for dense-interrogator environments

2.4 Proposed Architecture of the Reader Transceiver

In view of the above discussed system characteristics, a dual-conversion zero-IF architecture is adopted to eliminate the image-reject filter and to facilitate higher integration level with lower power consumption by making use of the DC-free FM0 and Miller-modulated subcarrier coding scheme. Compared with direct-conversion zero-IF, it has less problem with LO leakage and frequency pulling due to the fact that LO1, LO2 and RF are at different frequencies. In the proposed RFID reader, LO2 is chosen to be LO1 divided by two, therefore, the image of first down-conversion is located at around 300MHz, which can be rejected by the bandpass characteristic of antenna and LNA.

The signal reflected from tag to reader can use either ASK or PSK modulation, to

support both of them an IQ down-conversion architecture is implemented. For the transmitter side, in order to support Single-Side Band (SSB) ASK, IQ up-conversion are utilized too. Table 2.6 summarizes the derived system specification of the proposed RFID reader. Fig. 2.17 shows the transceiver architecture as well as the frequency plan.

Table 2.6 Derived system specification of the proposed RFID reader

System Specification	Value	
Frequency range	860MHz-960MHz	
Receiver bandwidth	80kHz to 1.28MHz	
Transmitter bandwidth	200 kHz for Europe	500 kHz for North America
BER	10^{-3}	
$SNR_{out\|max}$	11dB	
Listen mode sensitivity	-90dBm	
Listen mode noise figure @ 640kbps	12dB	
IIP3	-2dBm	
Maximum gain	95dB	
Phase noise of LO	-123dBc/Hz @ 1MHz	
Output power (w/o external PA)	8dBm	
Output power tuning range	20dB	
Output power (w external PA)	20dBm-27dBm	
ACPR	30dB	
Process	0.18μm CMOS	

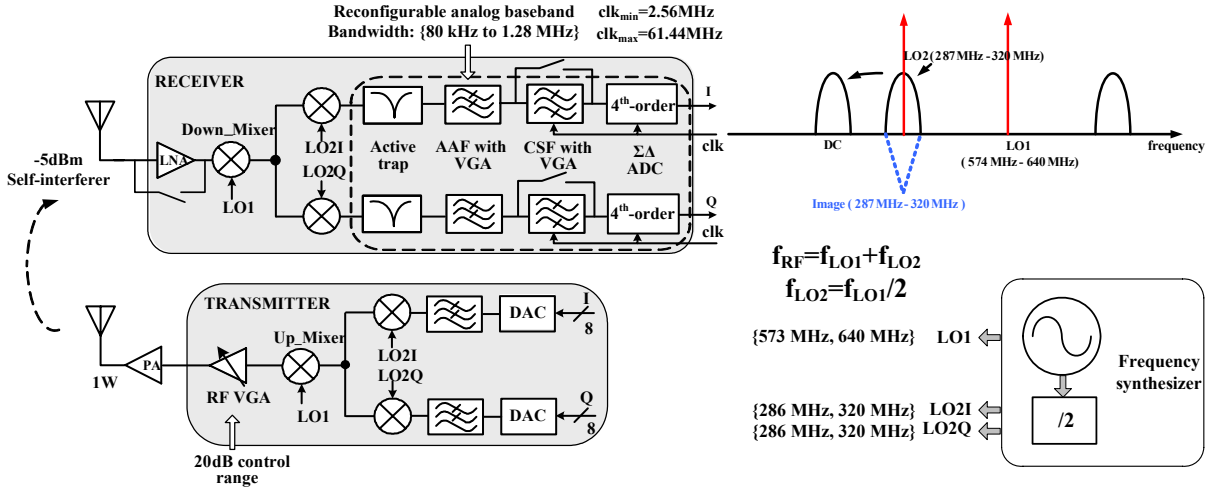


Fig. 2.19 Transceiver architecture and frequency plan

2.5 Features and Challenges

2.5.1 The Effect of Continuous Wave on Receiver Linearity and Sensitivity

Assuming that the output power from the transmitter is P_o and that the isolation between TX and RX is α dB, the self-interferer at the receiver input is about $(P_o–\alpha)$ dBm. For typical application, P_o is about 30dBm, while the α is 30-40dB by two separate antennas, it yields a CW as large as -10 to 0 dBm. Although, after down-conversion, the continuous wave will be located at DC and can be effectively blocked by the DC offset cancellation or AC coupling. High linearity of the RX front-end is mandatory in order to handle the large self-interferer, thus only limited gain can be implemented in the RX front-end to avoid saturation [10] [11].

The effects of the CW on the reader's receiver performance are not only saturating the receiver but also significantly increasing the input noise floor, hence reducing the receiver's SNR and degrading the sensitivity. The CW that the reader transmits is actually the LO signal amplified by the power amplifier. Therefore the CW has a finite spectrum purity which is quantified by LO phase noise. For a typical on-chip frequency synthesizer, the output spectrum is illustrated in Fig. 2.20.

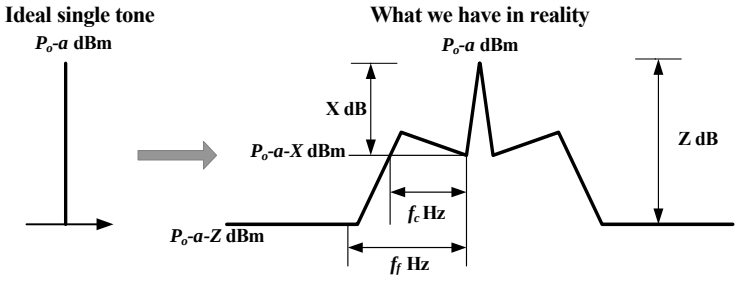


Fig. 2.20 Ideal and real continuous wave

The CW is not an ideal single tone, so it adds extra noise to the receiver. The receiver input noise floor NF_o and NF_{CW} without and with CW are given by (2-14) and (2-15).

$$NF_o = -174dBm + 10\log(BW) \tag{2-14}$$

$$NF_{CW} = P_o - \alpha + 10\log(\int_0^{BW} L_c(f)df) \tag{2-15}$$

where P_o–α is the power of the CW signal at the receiver's input, $L_c(f)$ is the phase noise of the CW at frequency offset f, and BW is the receiver baseband bandwidth. For largest BW=1.28MHz, with further assumption that the signals below 190 kHz are attenuated by AC coupling, the noise due to CW below 190 kHz is negligible. Thus in the frequency of interest, the synthesizer phase noise bears a $1/f^2$ relationship. As an example, if the phase noise is -123dBc/Hz@1MHz, then

$$L_C(f) = \frac{0.45}{f^2} \qquad 100kHz < f \le 1.28MHz \tag{2-16}$$

Plugging in some typical numbers: P_o=36dBm, NF_{sys}=12dB and α=40dB, the input noise floor due to the CW is calculated as:

$$NF_{in,CW} = 36 - 40 + 10\log[0.45 \times \left(\frac{1}{1.9 \times 10^5} - \frac{1}{1.28 \times 10^6}\right)] = -61dBm \tag{2-17}$$

while the input noise floor due to thermal noise is calculated as:

$$NF_{in} = -174 + 10\log(1.28M) = -113dBm \tag{2-18}$$

It is obvious that the input noise due to CW is much larger than the thermal noise. As a result, the system noise is dominated by the CW, and the sensitivity in the talk mode can be significantly degraded. As can be seen in (2-15), to reduce the CW-induced noise and minimize sensitivity degradation in talk mode, either the transmitting power P_o or its phase noise L_C has to be minimized, or the isolation between TX and RX α has to be maximized.

Reducing output power P_o will cause significant decrease in communication distance,

however, it can be very useful for a certain application when the desired communication distance is not too large; or when the system is operated in different countries with their own regulation on the maximum output power. Therefore it is imperative for a multi-protocol reader to have output power control. For the same antenna isolation α, reducing the output power P_o relaxes the linearity requirement of the front-end stages and increases the sensitivity of the system. On the other hand, it would be more desirable to keep the same output power thus communication distance, but maximize the isolation. However, the effects caused by coupling between antennas or circulators and substrate coupling in CMOS technology significantly limit the achievable isolation. Finally, the LO phase noise needs to be as low as possible, so the low phase noise on-chip frequency synthesizer becomes compulsory.

Because the noise is dominated by the CW in talk mode and the RX front-end cannot afford to have high gain to avoid saturation, in the proposed reader transceiver, LNA is bypassed in talk mode so that the linearity of later stages is relaxed a lot. Although this results in 16dB noise figure increase, thermal noise is still below the CW phase noise. In the listen mode without the CW, LNA is on and provide 16dB gain to enhance the listen mode sensitivity.

The CW is the distinctive feature of RFID system. To be able to receive the weak signal in the presence of a larger self-interferer makes the receiver linearity and noise much more challenging compared with other conventional wireless transceivers. It would be best if the self-interferer and its noise floor can be filtered to maintain the

RX linearity and sensitivity. However, present microwave technology fails to provide such a highly selective filter to reject the large blocker which is only a few hundred kHz away from the desired signal. A cancellation scheme is proposed in [12], where the blocker rejection is achieved through a combination of two RF paths. Nevertheless, the effectiveness of this technique highly depends on the phase difference between the blocker and the desired signal, which is virtually impossible to control in actual implementation. Moreover, for far field operation, effects such as multi-path phenomenon, reflection and absorption further deteriorate the achievable rejection. Novel technique is still required to handle this issue.

2.5.2 Multi-Protocol RFID Reader

Unlike other ordinary communication systems, the uplink and downlink in a RFID system is asymmetrical in terms of data encoding, date rate and modulation scheme. What's more, as can be seen from table 2.1, both the uplink and downlink features a variable data rate. For a given encoding and modulation scheme, the signal bandwidth will be varied according to data rate. As a result, it is optimal that the RFID reader would have a tunable bandwidth. In this way, both the RX sensitivity and selectivity can be optimized under different system bandwidth scenarios.

In addition to the self-interferer, in the dense-reader environment, interference can come from nearby working readers, which causes adjacent channel interference and further degrades the signal-to-interference ratio. Moreover, the capability to handle multiple protocols makes the adjacent interference rejection ability even more challenging. As an example, in Europe CEPT multi-channel regulatory environment,

10 channels of 200 kHz each in the range 865.6 MHz to 867.6 MHz are allocated. Readers talk in even-numbered channels, and tags backscatter in the odd-numbered ones. Consequently, the adjacent channel interference is expected to appear around 400 kHz offset. On the other hand, in North America, the transmitter's channel bandwidth is 500 kHz. Therefore, a multi-protocol reader that is able to dynamically minimize the power consumption while meeting all the multiple-protocol requirements in terms of data rates and dynamic range is highly desirable.

This work focuses on the implementation of a highly reconfigurable multi-protocol reader in terms of bandwidth, architecture, clock frequency, bias current, hence achieves optimal power dissipation for multi-protocol operation with different system bandwidth and interference scenarios.

2.5.3 Transmitter Characteristic

The transmitter is required to support DSB-ASK, SSB-ASK and PR-ASK as can be seen from table 2.1. It is realized by inputting different baseband data to the proposed reader transmitter as illustrated in Fig. 2.21.

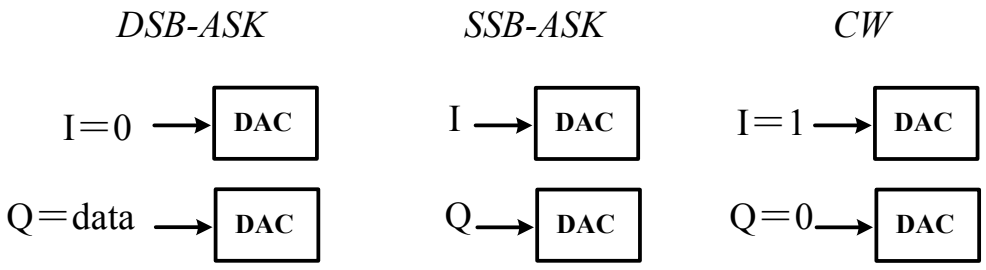


Fig 2.21 Generation of DSB-ASK, SSB-ASK and CW

Fig. 2.22 shows the simulated baseband output spectrum of PIE encoded DSB-ASK data. The transmitting signal has strong energy at DC. Therefore normal AC-coupling interface between DAC, TX-filter and up-mixer in the transmitter has to be avoided.

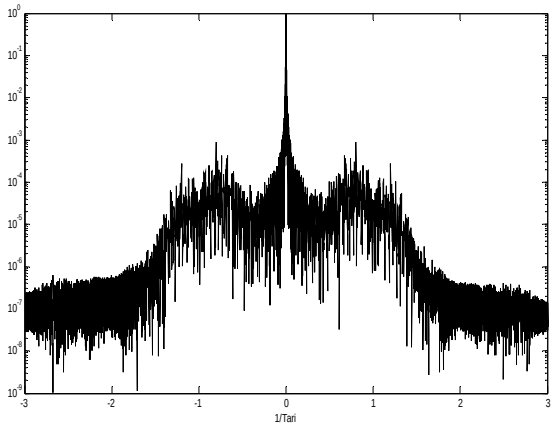


Fig 2.22 Simulated spectrum of baseband transmitting data

2.6 Specification of Building Blocks

After the system specification and architecture, the noise figure and IIP3 of cascaded building blocks can be calculated by Friis's formula (2-8) and (2-12).

It is worth mentioning again that one special feature of the proposed RFID reader is high input referred 1dB compression point of LNA and mixer due to the direct coupling of continuous wave from TX to RX. To avoid saturation, the front-end must have a very large input-referred 1dB compression point and cannot afford to have too much gain. Even in talk mode, with the LNA bypassed, the high linearity remains a big challenge of all the building blocks in RX. An active-trap is inserted between mixer and AAF, with a notch of about 12dB at adjacent interferer, the total linearity of the receiver can be improved by 8dB. Table 2.7 to 2.16 summarizes the derived specification of all building blocks in the reader transceiver.

Table 2.7 Specifications of LNA

LNA		
Frequency band	860MHz-960MHz	
Assumed output impedance(Ω)	200	
Gain (dB)	on	8 to 16

	bypass	0
NF@50Ω|$_{\text{max gain}}$ (dB)	on	5
	bypass	8
IIP3|$_{\text{Min gain}}$ (dBV)	on	-6
	bypass	0
Differential input 1dB compression point rms (dBV)	on	-33
	bypass	-13

Table 2.8 Specifications of down-conversion mixer

Down-conversion mixer	
Frequency band	RF: 860MHz-960MHz LO1: 574MHz-640MHz IF1=LO2: 287MHz-320MHz
Assumed input impedance(Ω)	3000
Assumed input impedance(Ω)	400
Gain (dB)	7
NF@50Ω|$_{\text{max gain}}$ (dB)	18
IIP3|$_{\text{Min gain}}$ (dBV)	0
Differential input 1dB compression point rms (dBV)	-13

Table 2.9 Specifications of AAF and VGA

AAF and VGA		
3-dB bandwidth	f_{upper}	80kHz to 1.3MHz
	f_{lower}	12~192kHz
Assumed input impedance (Ω)		4k
Assumed output impedance (Ω)		2k
Gain (dB)		3 to 58
NF@50Ω|$_{\text{max gain}}$ (dB)		18
Out-of-band IIP3|$_{\text{Min gain}}$ (dBV)		0
Attenuation		>62dB@32*f_{upper}

Table 2.10 Specifications of CSF and VGA

CSF and VGA		
3-dB bandwidth	f_{upper}	80kHz to 1.3MHz
	f_{lower}	12~192kHz
Assumed input impedance (Ω)		4k

Assumed output impedance (Ω)	2k
Gain (dB)	2 to 14
NF@50Ω$\|_{\text{max gain}}$ (dB)	37
Out-of-band IIP3$\|_{\text{Min gain}}$ (dBV)	5
Attenuation	>25dB@2*f_{upper}

Table 2.11 Specifications of ADC

ADC		
Input signal BW		80 kHz~1.28MHz
Oversampling ratio (OSR)		16 or 24
Maximum clk frequency		40.96MHz or 61.44MHz
Dynamic range@ max input BW	OSR=16	51dB
	OSR=24	70dB

Table 2.12 Specifications of Frequency synthesizer

Frequency Synthesizer	
Frequency band	860MHz-960MHz
Tuning range (LO1)	573MHz-640MHz
Tuning range (LO2)	287MHz-320MHz
Phase noise	-123dBc/Hz @ 1MHz
Spurious tone	-56dBc

Table 2.13 Specifications of DAC

DAC	
Input signal bandwidth	66 kHz to 256 kHz
No. of bits	8
F_{clk}	<20MHz

Table 2.14 Specifications of TX low pass filter

TX low pass filter	
3dB bandwidth	300 kHz
attenuation	30dB@5MHz
Gain (dB)	0
IIP3 (dBV)	10

Table 2.15 Specifications of up-conversion mixer

Up-conversion mixer	
Frequency band	LO1: 573MHz-640MHz LO2: 287MHz-320MHz
Assumed input impedance (Ω)	2k
Assumed output impedance (Ω)	200
Gain (dB)	-4
IIP3(dBV)	1

Table 2.16 Specifications of PA

PA	
Frequency band	860MHz-960MHz
Assumed input impedance (Ω)	200
$IIP3(dBV)\|_{max\ output\ power}$	-6
ACPR	30dBc
Input voltage	$0.1V_{pp\_single\_end}$
Output power	~8dBm
Gain tuning range	20dB

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Chapter 3
FRACTIONAL-N FREQUENCY SYNTHESIZER

3.1 Specification

Frequency synthesizer is required to have precise channel spacing, high frequency accuracy (10ppm to 20ppm) and low phase noise to meet the overall noise specification and to prevent unwanted signal mixing of the interferer. Low quality factor of the on-chip passive components make monolithic integration of a frequency synthesizer in standard CMOS technology a challenge. In the proposed RFID reader, one frequency synthesizer is required to generate LO1 and LO2 for both up and down frequency conversion.

The synthesizer specification can be derived according to the listen mode blocking profile specified in ETSI 302 208-1 regulation as shown in table 2.2 and graphically shown in Fig. 2.12

a) Phase noise: L{1 MHz}=(-87+35)-10log(1M)-11=-123dBc/Hz;

b) Spur: -87+35-11=-63dBc;

c) Switching time: in the order of milliseconds according to FCC part 15;

d) Frequency resolution: due to the unique asymmetrical uplink and downlink of the RFID system, the channel spacing will refer to the transmitter bandwidth in all the regulations and standards because it has a high output power. As

summarized in table 2.6, a minimal channel spacing of 100 kHz is required, which determines the frequency resolution of the frequency synthesizer.

e) Frequency tuning range: LO1 {573MHz-640MHz}; LO2 {286MHz – 320MHz}

Table 3.1 summarizes the derived specification of the proposed frequency synthesizer.

Table 3.1 Specification of the proposed frequency synthesizer

Specification	Value
Frequency tuning range	LO1: 573 MHz to 640 MHz
	LO2: 286 MHz to 320 MHz
Phase noise	-123dBc/Hz@1MHz
Spur	-63dBc
Switching time	<1ms
Frequency resolution	100kHz

3.2 System Design of the Frequency Synthesizer

3.2.1 Synthesizer architecture overview

A phase-locked loop (PLL) is a negative feedback system which is able to generate a stable clock as long as the reference signal is clean and stable. Therefore, reference frequency is typically implemented by a crystal controlled temperature compensated oscillator. There are three primary problems that challenge the PLL design. One is improving the frequency acquisition time or settling time. The second is reducing sidebands and spurious signals from appearing on the PLL's output. The third problem is the phase noise performance [1].

Since PLL-based frequency synthesizers are unanimously charge-pump PLL [2], all the discussion and analysis are based on this type of PLL. Three main kinds of PLL-based frequency synthesizers, integer-N PLL-FS, fractional-N PLL-FS and

dual-loop PLL-FS will be briefly introduced.

a) Integer-N PLL-FS

Fig. 3.1 depicts an integer-N frequency synthesizer. It consists of a voltage-controlled oscillator (VCO), a programmable divider, a phase-frequency detector (PFD), charge pump (CP) and loop filter (LF). The VCO generates an output signal that is dependent upon a DC control voltage at its input. The PFD senses the phase and frequency difference of the reference signal and divided down VCO signal, then generates "up" or "down" to drive the charge pump to charge or discharge the loop filter so as to control the VCO frequency.

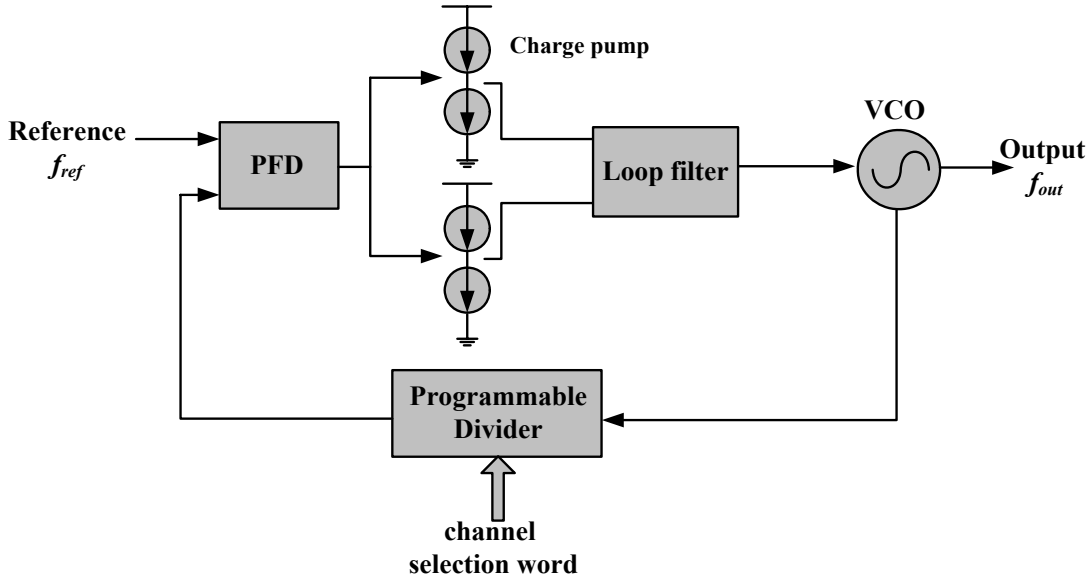


Fig. 3.1 Integer-N PLL frequency synthesizer

In an integer-N frequency synthesizer, the output frequency is integer multiple of the reference frequency

$$f_{out} = N \bullet f_{ref} \tag{3-1}$$

where division ratio N is an integer number. Therefore the frequency resolution of the integer-N frequency synthesizer is equal to the reference frequency f_{ref}. For narrow

band applications, it leads to a small reference frequency, consequently high division ratio in order to achieve high output frequency. Take GSM system for an example, the channel spacing equals to reference frequency of 200kHz, to generate 900MHz output the division ratio needs to be as large as 4500.

This inherent property of integer-N PLL-FS results in several disadvantages: First, since the loop bandwidth is usually smaller than one-tenth of the reference frequency for stability consideration, the settling time has to be sacrificed due to small loop bandwidth. Second, the reference spur and its harmonics are located at low offset frequencies. Third, the large division ratio *N* increases the in-band phase noise of the reference signal, the PFD, charge pump and frequency divider by *20log(N)* dB. Finally, with a small loop-bandwidth, the phase noise of VCO which shows a highpass characteristic will not be sufficiently suppressed at low offset frequencies. All these facts make the optimization difficult and the application of integer-N frequency synthesizer quite limited.

b) Fractional-N PLL-FS

Fractional-N frequency synthesizer circumvents the disadvantage of integer-N synthesizer by generating a fractional division ratio, so the reference frequency can be higher, consequently larger loop bandwidth and faster settling. However, the principle drawback of the fractional-N frequency synthesis is the unwanted low-frequency spurs due to the fixed pattern of the dual-modulus (or multi-modulus) divider. Various methods are proposed in the literature to suppress the fractional spurs to an acceptable level [3][4]. One of the most widely used types is ΣΔ

fractional-N frequency synthesizer as shown in Fig 3.2.

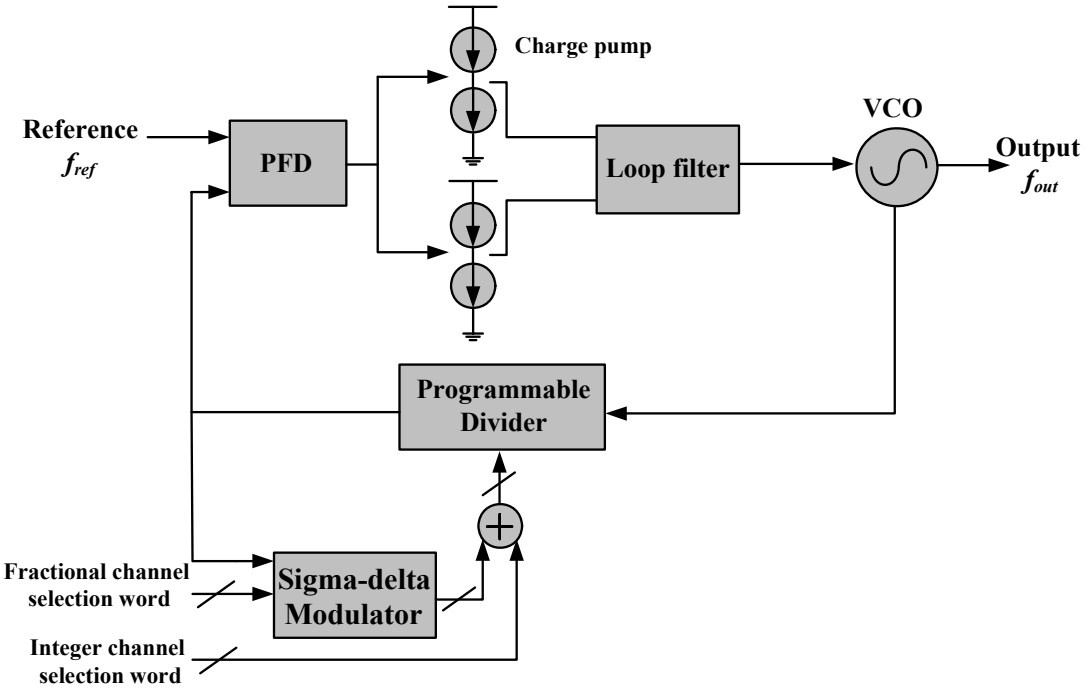


Fig. 3.2 Sigma-delta fractional-N frequency synthesizer

Noise and spurs are randomized and noise shaped to higher frequency offset through the sigma-delta modulator, and ultimately suppressed by the loop filter.

c) Dual-loop PLL-FS

To avoid the large division ratio in an integer-N frequency synthesizer, another alternative is to use multiple loops to reduce the division ratio. Dual-loop architecture is implemented to improve the tradeoff among phase noise, reference frequency, channel spacing and switching time [5][6]. However, dual-loop architecture requires two reference inputs, and at least on single sideband mixer, which might introduce additional spur and noise.

3.2.2 PLL Frequency Synthesizer Fundamental

By making the assumption that the PLL is continuous in time, basic feedback control theory utilizing Laplace Transform can be applied to determine the loop's behavior,

provided that the loop bandwidth is much less than the reference frequency. In practice it is true that the PFD and charge pump are not continuous in nature, so it is necessary to make this assumption in order to model the stability of the PLL using the Laplace Transform. When the loop bandwidth is wide, the sampling nature of the frequency divider and PFD cannot be ignored. The time delay of these devices will introduce phase shift (i.e., reduction in phase margin), thereby affecting the dynamic performance of the PLL. Another assumption is that the PLL has reached steady state. Under these assumptions, two models are valid which can be utilized to analyze the loop behavior, linear model and phase noise model.

a) Linear model

The block diagram of a simplified charge pump PLL frequency synthesizer is shown in Fig. 3.3. Fig 3.4 depicts the linear model, in which the building blocks are all represented by transfer functions. It is a popular method to characterize the PLL loop bandwidth, open-loop gain, closed-loop gain, stability and settling time.

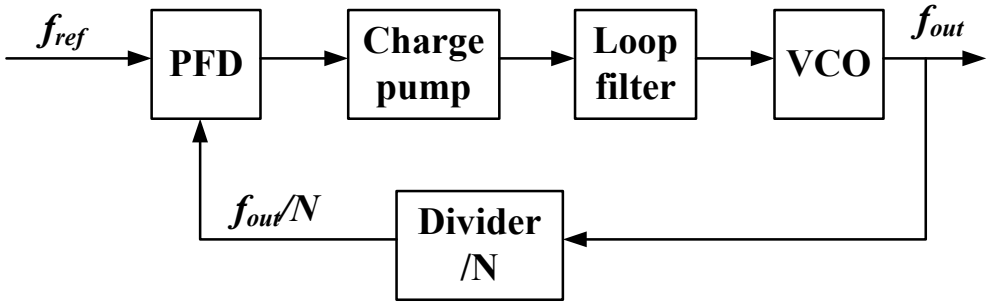


Fig. 3.3 Block diagram of charge pump PLL

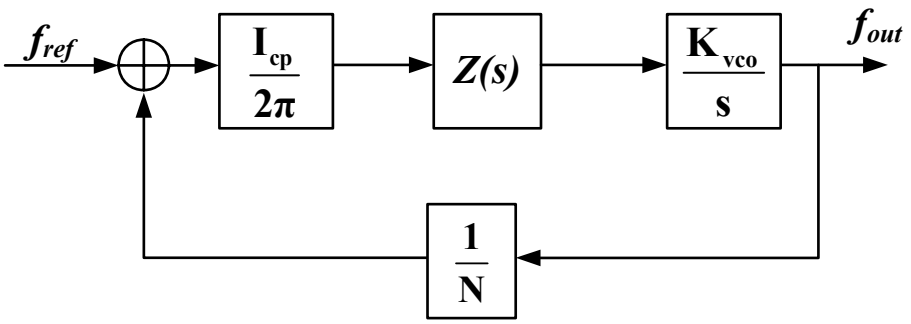


Fig. 3.4 Linear model

From Fig. 3.4, the open loop gain can be written as

$$G_o(s) = \frac{I_{cp} K_{VCO} Z(s)}{2\pi \cdot sN} \tag{3-2}$$

Where I_{cp} is the charge pump current (A), K_{VCO} is VCO gain (Hz/V), $Z(s)$ is the transimpedance of the loop filter, N is division ratio. The phase of the open loop gain can be expressed as

$$Phase = Phase(Z(s)) - 90^o \tag{3-3}$$

The open loop gain and phase transfer function are used in the analysis of the PLL's stability. The frequency at which the magnitude of the open loop response equals one is used to determine the stability of the PLL. As a measure of relative stability, the phase margin of the PLL is 180º plus the phase angle where the magnitude of the open loop response is equal to unity. The frequency at this point is referred to as the open loop bandwidth. For a stable PLL, the phase margin should be greater than 30º. Small phase margin would lead to peaking in the PLL's closed-loop response, therefore, usually 45º or 60º are preferable. The designers should make sure that the variations in the loop bandwidth, which occurs when a PLL is tuned, do not cause a loss in phase margin and affect the loop stability.

The closed-loop gain can be written as

$$G_{CL}(s) = \frac{G_0(s)}{1 + G_0(s)} \tag{3-4}$$

Assume a unit step function is applied to the PLL, the settling time is calculated by

$$f(t) = L^{-1}\{\frac{G_0(s)}{1 + G_0(s)} \cdot \frac{1}{s}\} \tag{3-5}$$

Most modern PLL falls into two categories: type I and type II. The type of system refers to the number of poles in the open loop gain located at the origin (i.e., the number of perfect integrators in the PLL). The order of the system refers to the degree of the characteristic equation or the denominator of the closed-loop transfer function. As shown in Fig. 3.4, there are two blocks that are a function of frequency, the loop filter and the VCO. Therefore, the loop filter *Z(s)* is the factor that determines the type and order of the PLL. Table 3.2 summaries the system phase error of type I and type II PLL.

Table 3.2 System phase error of type I and type II PLL

Input signal Φ_{ref}	Type I	Type II
Phase	0	0
Frequency	Constant	0
Time varying frequency	Continually increasing	Constant

b) Phase noise model

The phase noise performance is a critical parameter in the design of a PLL. The phase noise model discussed in this section is directed toward the identification of the major contributors to the overall phase noise in a PLL, and evaluating the relative contributions of the significant noise sources to the output power spectral density.

The term spectral density describes the energy distribution as a continuous function, expressed in units of phase variance per unit bandwidth. The spectral density is

described by the following equation

$$S_\phi(f_m) = \frac{\Delta\phi^2_{rms}(f_m)}{measurementBW} \tag{3-6}$$

The units of spectral density are rad^2/Hz. The U.S. National Bureau of Standards has defined the single sideband spectral density as

$$L(f_m) = \frac{P_{ssb}}{P_s} \tag{3-7}$$

where P_{ssb} is the power in one hertz of bandwidth at one phase modulation sideband and P_s is the total signal power. The single sideband spectral density $L(f_m)$ is directly related to the spectral density, $S_\phi(f_m)$, by

$$L(f_m) \cong \frac{1}{2} S_\phi(f_m) \tag{3-8}$$

This holds true only if the modulation sideband, P_{ssb}, is such that the total phase deviation is much less than 1 radian. $L(f_m)$ is expressed in dBc/Hz or dB relative to the carrier on a per hertz basis.

For the purpose of evaluating the noise performance of the PLL, each function blocks is considered noiseless and a noise signal is added into the PLL at the summing node of each building block as shown in Fig. 3.5.

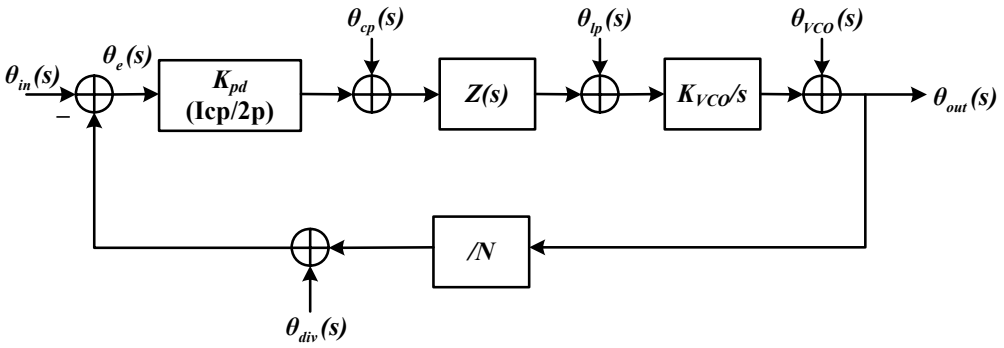


Fig. 3.5 Phase noise model

$\theta_{in}(s)$: input phase noise, contributed by the reference signal

K_{pd}: gain of PFD and charge pump, which is given by $I_{cp}/2\pi$ (A/rad)

$\theta_{cp}(s)$: charge pump noise

$\theta_{lp}(s)$: noise generated by the loop filter

$\theta_{VCO}(s)$: VCO phase noise

$\theta_{div}(s)$: phase noise of the frequency divider

$\theta_{out}(s)$: PLL output phase noise

The noise transfer function of each noise source with respect to the output is summarized in Table 3.3.

Table 3.3 PLL phase noise transfer function

Reference	$\theta_{out}(s)/\theta_{in}(s)$	$\frac{NG_0(s)}{1+G_0(s)}$	Lowpass
Charge pump	$\theta_{out}(s)/\theta_{cp}(s)$	$\frac{K_{VCO}Z(s)}{s}\bullet\frac{1}{1+G_0(s)}$	Lowpass
Loop filter	$\theta_{out}(s)/\theta_{lp}(s)$	$\frac{K_{VCO}}{s}\bullet\frac{1}{1+G_0(s)}$	Bandpass
VCO	$\theta_{out}(s)/\theta_{VCO}(s)$	$\frac{1}{1+G_0(s)}$	highpass
Divider	$\theta_{out}(s)/\theta_{div}(s)$	$-\frac{NG_0(s)}{1+G_0(s)}$	lowpass

Then the total phase noise of the PLL output at offset frequency $\Delta\omega$ is

$$N_{out}(\Delta\omega)=\left|H_{ref}\right|^2 N_{ref}+\left|H_{cp}\right|^2 N_{cp}+\left|H_{lp}\right|^2 N_{lp}+\left|H_{VCO}\right|^2 N_{VCO} \tag{3-9}$$

Where H_i denotes the noise transfer function, N_i is the power spectral density that is a function of the offset frequency $\Delta\omega$ from the carrier.

As can be seen from Table 3.3, the phase noise inside the loop bandwidth is multiplied by reference noise and divider noise, while the noise outside the loop

bandwidth is primarily that of the VCO.

3.2.3 Proposed Frequency Synthesizer Architecture

Given the specification, a channel spacing of 100 kHz necessitates the use of a fractional-N frequency synthesizer rather than an integer-N one. As discussed in section 3.2.1 ΣΔ fractional-N frequency synthesis can circumvent the severe speed-spectral purity-resolution tradeoff by synthesizing fractional multiples of the reference frequency. The fractional spurs are randomized and noise shaped by the ΣΔ action and ultimately filtered by the loop filter [7].

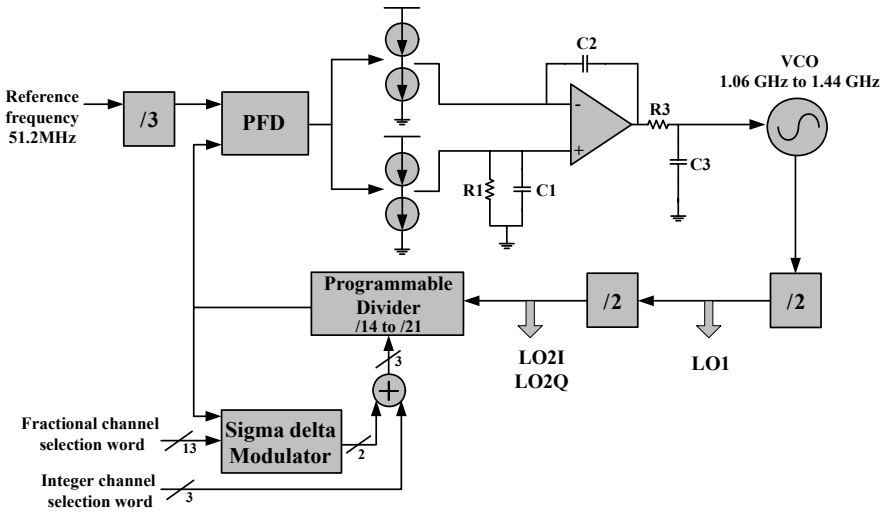


Fig. 3.6 Architecture of the proposed fractional-N frequency synthesizer

Fig. 3.6 illustrates the system architecture of the proposed fractional-N frequency synthesizer. It comprises an LC VCO operating around 1.2 GHz, 2 divide-by-two circuits, a programmable divider controlled by ΣΔ modulator; PFD, two charge pumps, and a type II 3rd-order dual-path loop filter to minimize the on-chip capacitance and chip area. The LC VCO is designed to operate at twice the desired LO1 frequency to minimize the inductance and the chip area without sacrificing its quality factor Q. In addition, LO1 phase noise is improved by 6 dB due to the

divide-by-2 circuit following the VCO. A divide-by-3 after the reference input generate accurate channel spacing as f_{LO1} is 2/3 of f_{RF} in the proposed synthesizer, moreover, it helps to lower the phase noise of the reference source. The proposed VCO is modified from the transformer-feedback VCO [8] to achieve low phase noise under low supply voltage. A 3rd-order single-loop sigma-delta modulator is employed to produce two noise-shaped output bits to represent the fractional part of the channel-selection word and to control the programmable divider together with 3 bits for the integer part.

3.2.4 System Design

After the synthesizer architecture is chosen, next step is to perform system calculation and behavior simulation by making use of the linear model and phase noise model. Various design parameters and loop filter component values are to be determined first. Then system simulation or calculation is carried out to check the loop stability, switching time and phase noise.

a) Loop filter component calculation

The schematic of the dual-path loop filter is redrawn in Fig 3.7. The transimpedance is calculated as

$$Z(s) = \frac{V_c}{i_{cp}} = \frac{1}{sC_2} \cdot \frac{1 + sR_1(C_1 + B \cdot C_2)}{1 + sR_1C_1} \cdot \frac{1}{1 + sR_3C_3} \tag{3-10}$$

Further define

$$\tau_Z = R_1(C_1 + B \cdot C_2) \approx R_1BC_2 \tag{3-11}$$

$$\tau_{p1} = R_1C_1 \tag{3-12}$$

$$\tau_{p3} = R_3C_3 \tag{3-13}$$

Substituting (3-11), (3-12), (3-13) into (3-10) results in

$$Z(s) = \frac{1}{sC_2} \cdot \frac{1+s\tau_Z}{1+s\tau_{p1}} \cdot \frac{1}{1+s\tau_{p3}} \tag{3-14}$$

Substitute (3-14) into (3-2), we have

$$G_o(s) = \frac{I_{cp}K_{VCO}}{2\pi \cdot NC_2} \cdot \frac{1+s\tau_Z}{s^2\left(1+s\tau_{p1}\right)} \cdot \frac{1}{1+s\tau_{p3}} \tag{3-15}$$

Or

$$G_o(j\omega) = \frac{I_{cp}K_{VCO}}{2\pi \cdot NC_2} \cdot \frac{1+j\omega\tau_Z}{-\omega^2\left(1+j\omega\tau_{p1}\right)} \cdot \frac{1}{1+j\omega\tau_{p3}} \tag{3-16}$$

The open loop phase response and phase margin are given by

$$Phase(G_o) = -180^o + \arctan(\omega\tau_Z) - \arctan(\omega\tau_{p1}) - \arctan(\omega\tau_{p3}) \tag{3-17}$$

$$PM = \tan^{-1}\left(\omega\tau_Z\right) - \tan^{-1}\left(\omega\tau_{p1}\right) - \tan^{-1}\left(\omega\tau_{p1}\right) \tag{3-18}$$

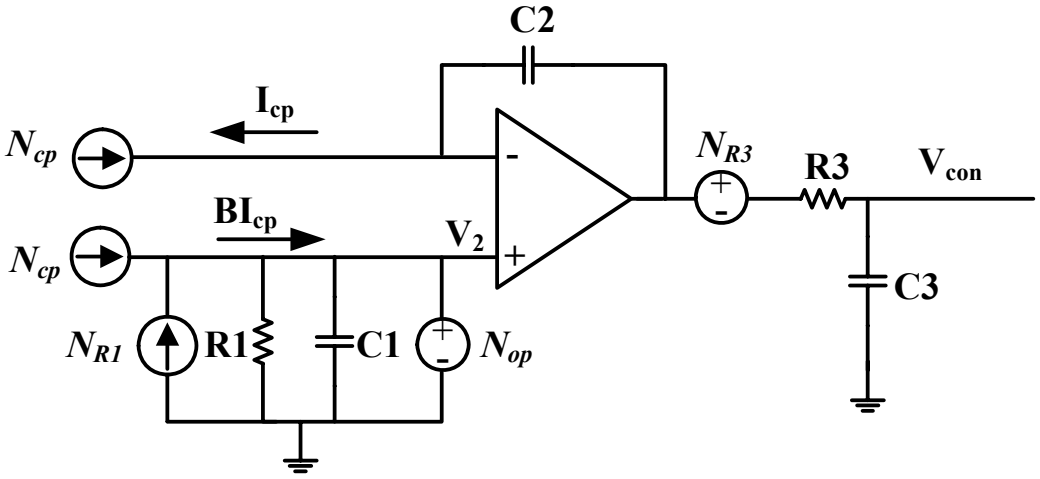


Fig. 3.7 Schematic of the dual-path loop filter

One way to design the loop filter component is make sure the largest phase margin occurs at the crossover frequency ω_c as illustrated in Fig. 3.8. Further assume $\tau_{p1}=\tau_{p3}$. Thus for a target phase margin of 60º, following relationship holds

$$\begin{cases} \dfrac{dPhase(\omega_c)}{d\omega} = 0 \\ \left|G_0(j\omega_c)\right| = 1 \\ PM\big|_{\omega_c} = 60^o \\ \tau_{p1} = \tau_{p3} \end{cases} \tag{3-19}$$

Substituting (3-16), (3-17), (3-18) into (3-19) and solving the above equations, we can obtain the loop filter component value. An alternative approach is described in [9]. All the component values are derived by making some empirical assumption and simplification.

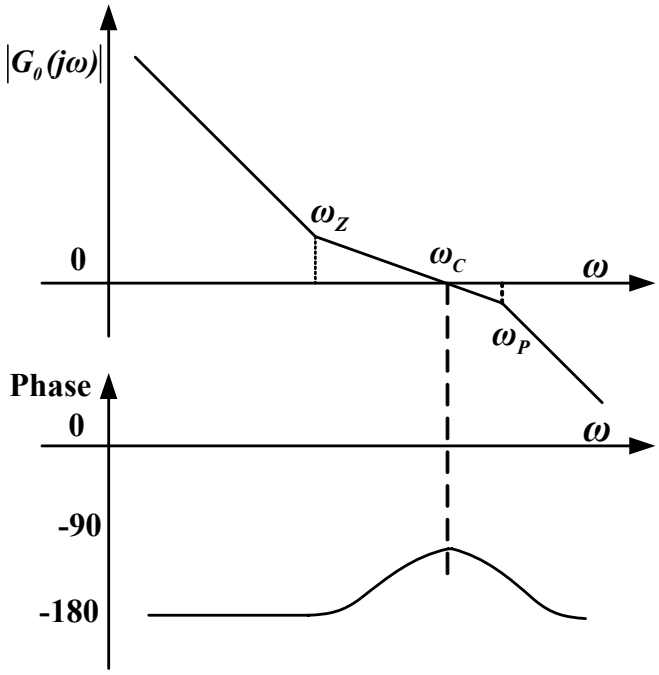


Fig. 3.8 Calculation of loop filter component

Table 3.4 compares analytical and numerical results of the two methods for deriving the dual-path loop filter component values. For the proposed synthesizer, following parameters are adopted: K_{vco}=8MHz/V; Loop bandwidth=30kHz; N=37.5; I_{cp}=2uA; B=30, K_{c13}=1.5. Fig 3.9 illustrates the calculated open loop gain and phase response of the proposed fractional-N frequency synthesizer. Fig 3.10 shows the step response.

Settling time is about 80μs.

Table 3.4 Comparison of two approaches for loop filter calculation

	First approach		Approach in [9]	
R1	$\frac{2\pi\omega_c^2 N(\tau_z-\tau_p)}{BI_{cp}K_{VCO}}\cdot\frac{1+(\omega_c\tau_p)^2}{\sqrt{1+(\omega_c\tau_z)^2}}$	13.9kΩ	$\frac{2\pi N\omega_c}{I_{cp}K_{VCO}B}$	14.7kΩ
C1	$\frac{\tau_p BI_{cp}K_{VCO}}{2\pi\omega_c^2 N(\tau_z-\tau_p)}\cdot\frac{\sqrt{1+(\omega_c\tau_z)^2}}{1+(\omega_c\tau_p)^2}$	49.2pF	$\frac{I_{cp}K_{VCO}B}{12\pi N\omega_c^2}$	60pF
C2	$\frac{I_{cp}K_{VCO}}{2\pi\omega_c^2 N}\cdot\frac{\sqrt{1+(\omega_c\tau_z)^2}}{1+(\omega_c\tau_p)^2}$	44.8pF	$\frac{2I_{cp}K_{VCO}}{\pi N\omega_c^2}$	48.1pF
R3	$\frac{R_1}{K_{c13}}$	9.3kΩ	$\frac{R_1}{K_{c13}}$	9.8kΩ
C3	$K_{c13}C_1$	73.8pF	$K_{c13}C_1$	90.2pF

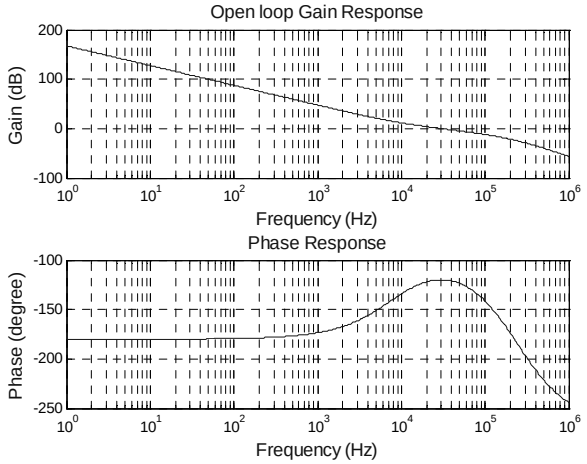


Fig. 3.9 Calculated open loop gain and phase response of the proposed synthesizer

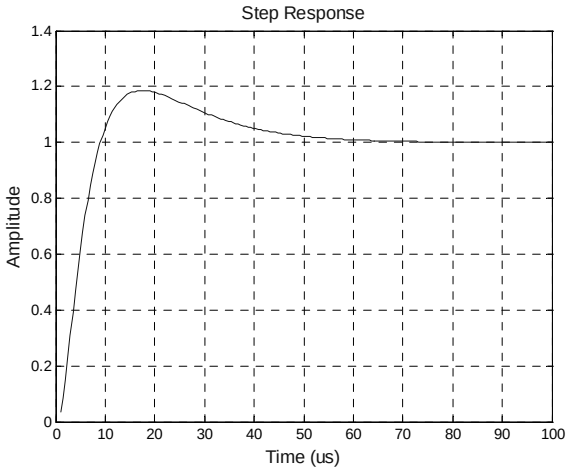


Fig. 3.10 Step response of the proposed synthesizer

To ensure the stability against all the frequency corners, Hspice behavior simulation is performed as shown in Fig. 3.11 [9]. The loop filter component values are fixed, while the VCO gain and division ratio are varied to check the phase margin over the designed frequency tuning range.

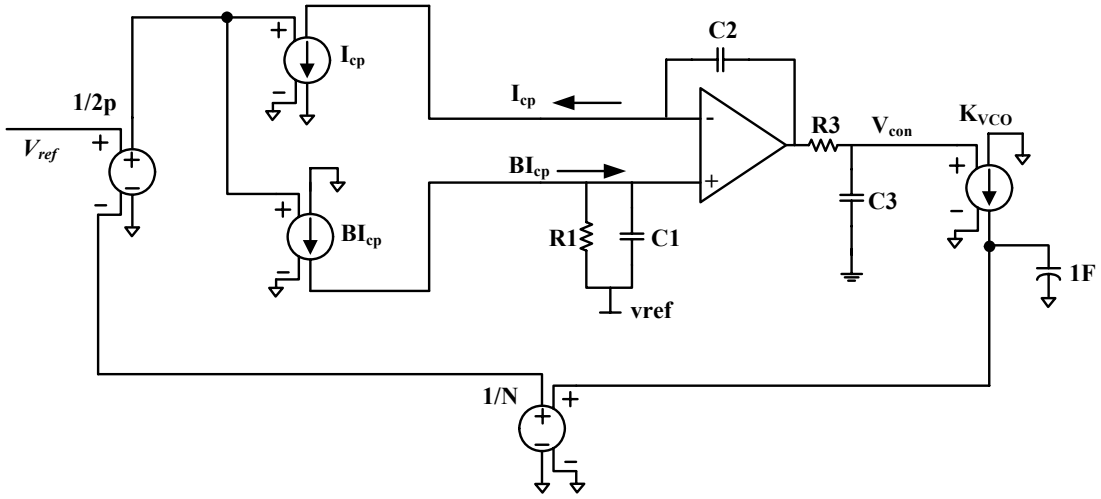


Fig. 3.11 Hspice behavior simulation

b) Noise calculation

Noise model introduced in 3.2.2 is utilized to calculate the phase noise of the proposed synthesizer. We first analyze the noise contribution of the dual-path loop filter. The noise of the loop filter is contributed by charge pump, opamp, resistor R1

and R3 as shown in Fig 3.7. To calculate the noise contribution of each component, we first define the following transfer function

$$H_1(s) = \frac{R_1}{s\tau_{p1} + 1} = \frac{R_1}{sR_1C_1 + 1} \tag{3-20}$$

$$H_3(s) = \frac{1}{s\tau_{p3} + 1} = \frac{1}{sR_3C_3 + 1} \tag{3-21}$$

$$V_2 = BI_{cp}H_1(s) + \frac{I_{cp}}{sC_2} \Rightarrow \frac{V_2}{I_{cp}} = BH_1(s) + \frac{1}{sC_2} \tag{3-22}$$

$$H_3(s) = \frac{V_c}{V_2} \tag{3-23}$$

Opamp noise is calculated as

$$L_{op} = \frac{1}{2} N_{op} \left(\frac{K_{VCO} \cdot H_3(s)}{s \cdot (1 + G_0(s))} \right)^2 \tag{3-24}$$

where $N_{op(s)}$ is the input referred voltage noise of the opamp in unit of V^2/Hz.

Resistor R3 noise is modeled as a voltage noise and can be calculated as

$$\begin{aligned} L_{R3} &= \frac{1}{2} 4kTR_3 \left(\frac{K_{VCO} \cdot H_3(s)}{s \cdot (1 + G_0(s))} \right)^2 \\ &= 4kT \frac{\pi\omega_c^2 N(\tau_z - \tau_p) K_{VCO}}{K_{c13} BI_{cp}} \cdot \frac{1 + (\omega_c\tau_p)^2}{\sqrt{1 + (\omega_c\tau_z)^2}} \left(\frac{H_3(s)}{s \cdot (1 + G_0(s))} \right)^2 \end{aligned} \tag{3-25}$$

Noise contribution of Resistor R1 is modeled as a current noise at the V_2 and can be written as

$$\begin{aligned} L_{R1} &= \frac{1}{2} \frac{4kT}{R_1} \left(\frac{K_{VCO} \cdot H_3(s) H_1(s)}{s \cdot (1 + G_0(s))} \right)^2 \\ &= kT \frac{BI_{cp} K_{VCO}}{\pi\omega_c^2 N(\tau_z - \tau_p)} \cdot \frac{\sqrt{1 + (\omega_c\tau_z)^2}}{1 + (\omega_c\tau_p)^2} \left(\frac{K_{VCO} \cdot H_3(s) H_1(s)}{s \cdot (1 + G_0(s))} \right)^2 \end{aligned} \tag{3-26}$$

The noises of the charge pump are derived as

$$L_{CP} = \frac{1}{2} N_{CP} \left[B(H_1(s))^2 + (\frac{1}{sC_2})^2 \right] \left(\frac{K_{VCO} H_3(s)}{s \cdot (1 + G_0(s))} \right)^2$$
$$= \frac{1}{2} 4kT \cdot \frac{2}{3} \cdot g_m \cdot \lambda_{on} \cdot \left[B(H_1(s))^2 + (\frac{1}{sC_2})^2 \right] \left(\frac{K_{VCO} H_3(s)}{s \cdot (1 + G_0(s))} \right)^2 \quad (3\text{-}27)$$

where λ_{on} is the switch-on duty cycle of the charge pumps.

As shown in Table 3.3, the noise of VCO and reference are

$$L_{VCO} = N_{VCO} \left(\frac{1}{1 + G_0(s)} \right)^2 \quad (3\text{-}28)$$

$$L_{ref} = \frac{1}{2} N_{ref} \left(\frac{N G_0(s)}{1 + G_0(s)} \right)^2 \quad (3\text{-}29)$$

For ΣΔ fractional-N frequency synthesizer, quantization noise L_{SD} needs to be modeled as well, which will be discussed in section 3.3.2. After derivation of all the noise contributions, the total phase noise of the PLL can be expressed as

$$L_{PLL}(s)\big|_{s=j\omega} = L_{VCO}(s) + L_{ref}(s) + L_{SD}(s) + L_{CP}(s) + L_{R1}(s) + L_{R3}(s) + L_{op}(s) \quad (3\text{-}30)$$

When the stability, settling time and phase noise are all satisfied, system design is completed. Normally several iterations are required to achieve optimization and meet all the specifications. The next step in the synthesizer design is circuit level implementation.

3.3 Circuit Implementation

3.3.1 VCO

There are two basic types of on-chip VCO's for high frequency PLL: the ring oscillator and the LC-tuned oscillator. The ring oscillator consists of a number of delay cells. It occupies less area and has a large tuning range. The LC oscillator takes more chip area due to on-chip spiral inductors and exhibits less tuning capability, but

it is more suitable for high frequency operation and generally has much better phase noise compared with ring oscillator. In the RFID synthesizer, low phase noise requirement makes the LC-VCO more preferable.

a) LC-VCO Fundaments

A resonator contains an inductor, capacitor and resistor as shown in Fig. 3.12. The neutral oscillation frequency is mainly determined by inductor and capacitor and is given as

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{3-31}$$

To ensure continuous oscillation, loss in the LC-tank should be cancelled. Therefore a negative resistance is added to compensate the energy loss which is usually implemented by cross-coupled pairs. Fig 3.13 shows the schematic of a typical voltage controlled oscillator.

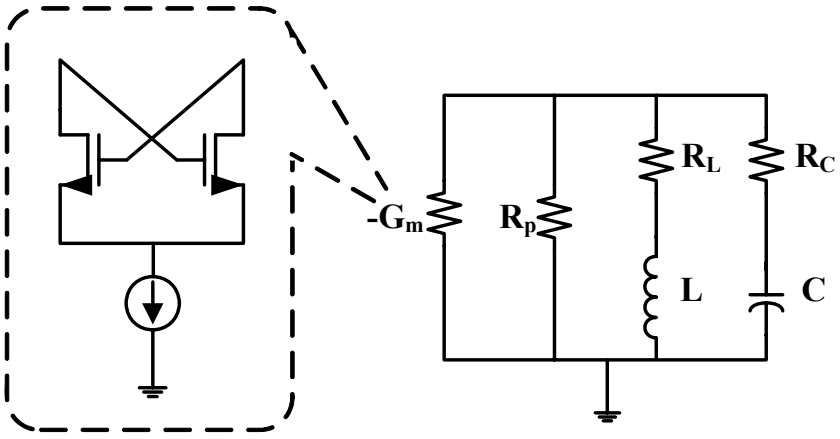


Fig. 3.12 Lossy LC tank with negative tank

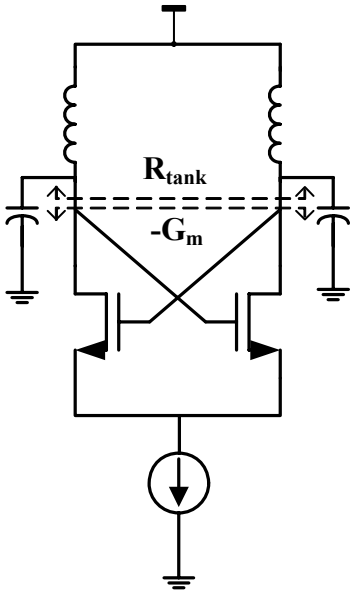


Fig. 3.13 Schematic of NMOS VCO

The quality factor of the inductor is defined as

$$Q_L = \frac{\omega L}{R} \tag{3-32}$$

Generally, with on-chip passive elements, the loss in the LC tank is mainly contributed by the integrated inductor rather than the capacitors. In order to provide enough energy to start oscillation, the transconductance of the NMOS in Fig. 3.13 is at least [9]

$$g_m = \frac{2R_{\tan k}}{(\omega_o L)^2} \tag{3-33}$$

To guarantee oscillation, in actual design, g_m is usually designed to be two time larger than the value given by (3-33). The power of the oscillator is

$$power = 2IV_{dd} \tag{3-34}$$

where the current I is given by

$$I = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 = \frac{g_m}{2}(V_{GS} - V_T) \tag{3-35}$$

Substituting (3-31) and (3-35) into (3-34) results in

$$power \propto V_{dd} R_{\tan k} \frac{C}{L} \tag{3-36}$$

It is shown that to minimize the power of VCO, the ratio of C/L should be minimized.

b) Inductors and transformers

Of all the passive structures used in RF circuits, high-quality inductors and transformers or baluns are the most difficult to realize monolithically. In silicon, they suffer from three parasitic effects [10]. First, parasitic capacitance to the substrate causes the inductor to self-resonate at a certain frequency. Second, the high frequency series resistance will differ from the calculated one due to skin effect and other magnetic field effects. Third, the losses in the heavily doped substrate cause a large degradation in the overall quality factor and reduce the inductance value. Therefore, inductors made in silicon technology with aluminum interconnect typically exhibits a quality factor (Q) of 5. Over the past few years much research has been done in efforts to improve fabrication methods and modeling accuracy.

Bondwires can be used as inductor. Compared with spiral inductors, bondwire inductor has a superior Q. However, the main drawback is large spread of their values, lack of reproducibility and difficulty to be accurately controlled.

Fig 3.14 shows a basic π model of on-chip inductor. A number of nonideal components are added to account for various parasitics. R_s models the series resistance of the metal lines used to form the inductor. Note that R_s will increase at higher frequency due the skin effect. C_{ox} models the capacitance from the metal lines to the substrate. This is essentially a parallel-plate capacitor formed between the

inductor metal and the substrate. C_{sub} and R_{sub} models the losses due to magnetic effects, capacitance and the conductance of the substrate. C_{IW} models the inter-winding capacitance between the traces. This is another parallel-plate capacitor formed by adjacent metal lines.

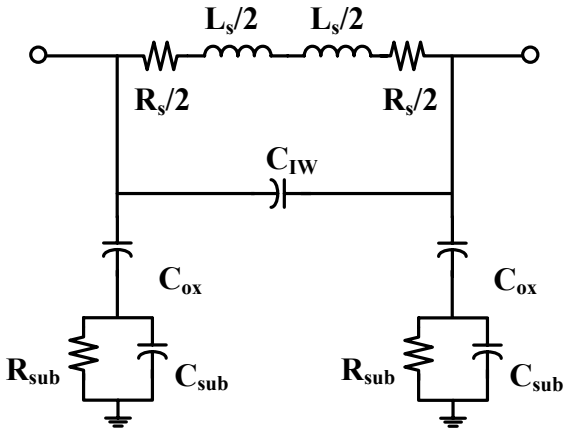


Fig. 3.14 Inductor π model

Integrated transformers have been found useful in varieties of applications [11] [12]. The operation of a passive transformer is based upon the mutual inductance between two or more conductors, or windings. The transformer is designed to couple alternating current from one winding to the other without a significant loss of power, and impedance levels between the windings are transformed in the process. As shown in Fig. 3.15(a), magnetic flux produced by current i_p flowing into the primary winding at terminal *P* induces a current in the secondary winding that flows out of terminal *S*. This produces a positive voltage v_s across a load connected between terminals *S*+ and *S*-. The main electrical parameters of interest to a circuit designer are the transformer turns ratio *n* and the coefficient of magnetic coupling *k*. The current and voltage transformations between windings in an ideal transformer are related to the turns ratio by the following equation:

$$n = \frac{v_S}{v_P} = \frac{i_P}{i_S} = \sqrt{\frac{L_S}{L_P}} \tag{3-37}$$

where the v_p and v_s, i_p and i_s stand for primary and secondary voltages and currents. L_p and L_s are the self-inductances of the primary and secondary coils respectively. The magnetic coupling between windings is indicated by the coupling factor

$$k = \frac{M}{\sqrt{L_P L_S}} \tag{3-38}$$

where M is the mutual inductance between the primary and secondary windings. The self-inductance of a given winding is the inductance measured at the transformer terminals with all other windings open-circuited. Fig 3.15(b) shows a T model of transformer which uses three inductors to model the mutual coupling between windings. This model simplifies hand analysis of circuits incorporating transformers. However, it is only valid for ac signals because there must be isolation of dc current flow between the primary and secondary loops in a physical transformer.

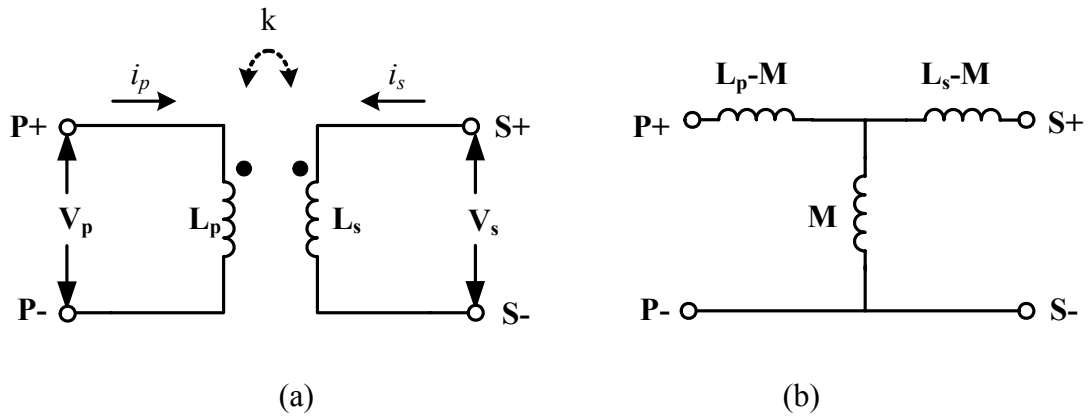


Fig. 3.15 Monolithic transformer (a) Schematic symbol (b) T model

c) LC-VCO phase noise

The oscillator's phase noise model was heuristically deduced by Leeson [13]. It is based on a linear time-invariant (LTI) approach for tuned tank oscillators. It predicts

the following behavior for $L\{\Delta\omega\}$

$$L\{\Delta\omega\} = 10\log\{\frac{2FkT}{P_s}[1+(\frac{\omega_0}{2Q_L\Delta\omega})^2](1+\frac{\omega_{1/f^3}}{|\Delta\omega|})\} \tag{3-39}$$

where F is an empirical parameter (often called the "device excess noise factor"), k is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q_L is the effective quality factor of the tank with all loadings accounted for (also known as loaded Q), $\Delta\omega$ is the offset from the carrier, and ω_{1/f^3} is the frequency of the corner between the $1/f^3$ and $1/f^2$ region.

Unfortunately, it is generally difficult to calculate F a priori. One important reason is that much of the noise in a practical oscillator arises from periodically time-varying processes which are not properly treated in an LTI context. Hence, F is usually an a posteriori fitting parameter derived from measured data.

To sustain oscillation, the average energy provided by the tank by the active device should be equal to the energy losses in the resonant circuit as shown in Fig. 3.12. The total equivalent parallel resistance of the tank has an equivalent mean square noise current density of $i_n^2/\Delta f = 4kTG_m$ .Using the effective noise current power, the phase noise in the $1/f^2$ region of the spectrum can be calculated as

$$L\{\Delta\omega\} = 10\log\{\frac{2FkT}{P_s}(\frac{\omega_0}{2Q_L\Delta\omega})^2\} \tag{3-40}$$

Recently, a more accurate time-variant phase noise model has been developed for oscillator [14]. The function, $\Gamma(x)$, is the time-varying "proportionality factor". It is called the impulse sensitivity function (ISF), since it determines the sensitivity of the

oscillator to an impulsive input. It is a dimensionless, frequency-and amplitude-independent function periodic in 2π that describes how much phase shift results from applying a unit impulse at any point in time. The ISF for an ideal LC oscillator with a cosine waveform is a sine function. It should also be noted that the linearity and time-variance of a system depends on both the characteristics of the system and its input and output variables. The phase noise can be estimated by

$$L\{\Delta\omega\} = 10\log\{\frac{\Gamma_{rms}^2}{q_{\max}^2}\cdot\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\} \tag{3-41}$$

where $\overline{i_n^2}/\Delta f$ is input noise current power spectrum density (voltage mean-square density per unit bandwidth), Γ_{rms}^2 is the rms value of Γ(x), $q_{\max} = C_{node}V_{\max}$ is the maximum charge swing and V_{max} is the voltage swing across the capacitor caused by the current impulse. This equation gives the phase noise spectrum of an arbitrary oscillator in the $1/f^2$ region of the phase noise spectrum.

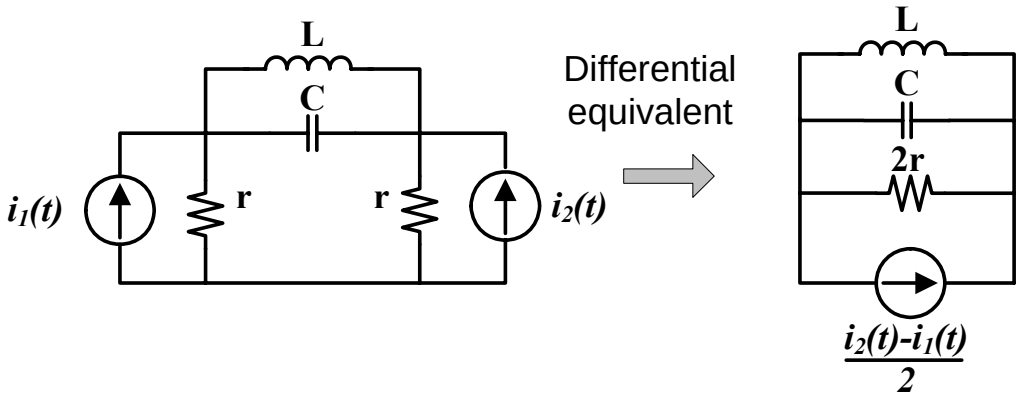


Fig. 3.16 Simplified model for transistor noise sources in a differential LC oscillator

In an NMOS differential LC oscillator, the equivalent noise circuit mode is shown in Fig. 3.16. The total noise power due to the active transistor can be expressed as

$$\overline{i_n^2}/\Delta f = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS}-V_T) = 4kT\gamma g_m \tag{3-42}$$

where μ is the mobility of the carriers in the channel, C_{ox} is the oxide capacitance per unit area, W and L are width and length of the MOS transistor. γ is around 2/3 for long channel transistors while it may be between 2 and 3 in the short channel region. In addition, the contribution of effective series resistance of the inductor, r_s, caused by ohmic losses in metal and substrate is given by

$$\overline{i_{rs}^2} / \Delta f = 4kT \frac{r_s}{L} C = \frac{4kT}{R_p} \tag{3-43}$$

where $R_p=Q^2 r_s=(L\omega_0)^2/r_s$ is the equivalent parallel resistance at the frequency of oscillation. Substitute (3-42) and (3-43) into (3-41), the total phase noise is

$$L\{\Delta\omega\} = 10\log\{\frac{2\Gamma_{rms}^2}{q_{\max}^2 \Delta\omega^2}[kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS}-V_T) + kT\frac{r_s}{L}C]\} \tag{3-44}$$

d) Modified-transformer feedback VCO

For low voltage operation, transformer feedback VCO proposed in [8] is a good candidate. Due to the extra voltage swing and extra positive feedback mechanism provided by the transformer coupling, it has the potential of low voltage and lower power consumption for given phase noise. Moreover, coupled resonators exhibit an enhanced quality factor Q thanks to the second-order band-pass nature [15]. In order to combine these favorable features for low power and low phase noise, the capacitances at the drain and source in the transformer-feedback VCO are optimally designed. Fig. 3.17 shows the schematic of the proposed VCO together with the coupled resonator model. The impedance at primary coil is calculated to be:

$$Z_{11} = \frac{s^3(L_pC_sL_s - C_sM^2) + s^2(L_pR_sC_s + C_sL_sR_p) + s(R_sR_pC_s + L_p) + R_p}{s^4(L_pC_pC_sL_s - C_pC_sM^2) + s^3(L_pR_sC_sC_p + C_pC_sL_sR_p) + s^2(R_sR_pC_sC_p + L_pC_p + C_sL_s) + s(C_pR_p + R_sC_s) + 1} \tag{3-45}$$

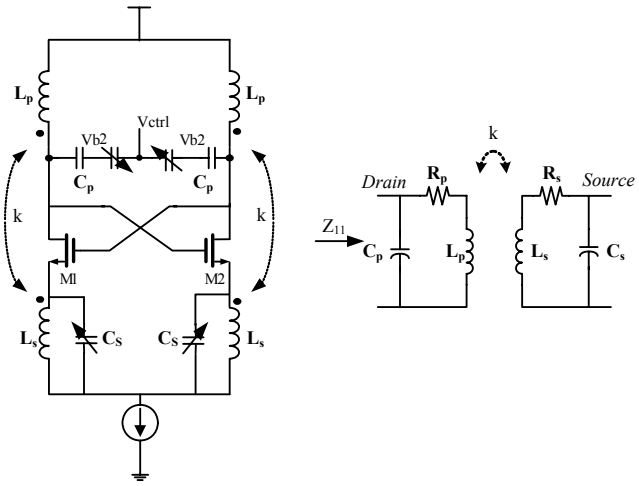


Fig. 3.17 Schematic of the proposed VCO

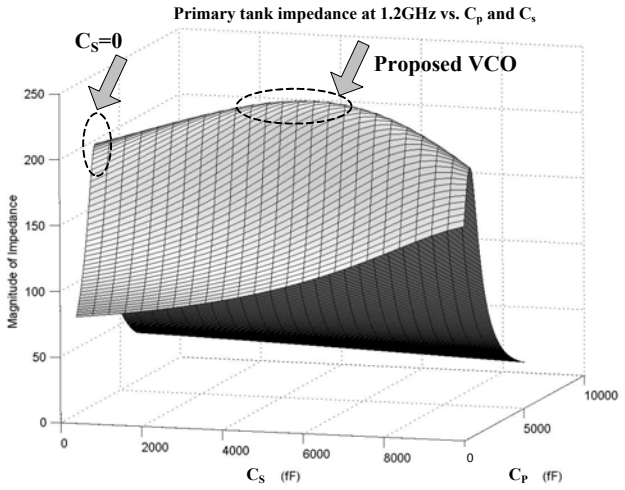


Fig. 3.18 Primary tank impedance versus capacitance C_p and C_s

As shown in Fig. 3.18, for given transformer's design parameters, namely L_p, L_s, k, there exists an optimal pair of C_p and C_s that provides the largest tank impedance Z_{11} at a given frequency. An increase in tank impedance is desirable because it offers larger oscillation amplitude and thus lower phase noise. Moreover, by designing the secondary coil at source to resonate at a frequency close to 2nd harmonic of oscillation frequency, the proposed VCO can provide additional noise filtering of even harmonics, which further helps to lower phase noise. Fig. 3.19 illustrates the impedance at source with Q of 5 at primary and secondary coils for two different C_s,

while other parameters of the couple resonator remain the same.

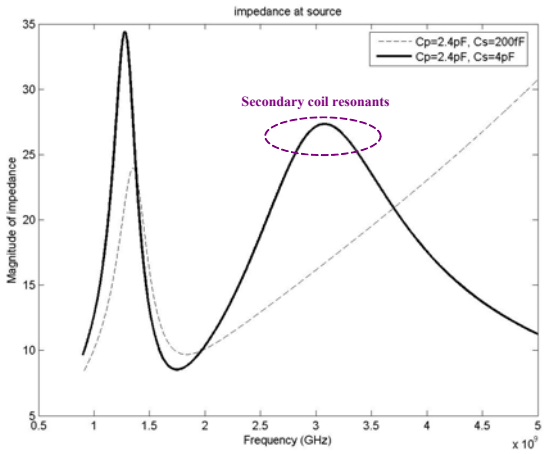


Fig. 3.19 Impedance at source node for two source capacitance

In order to meet the overall low phase noise requirement of the frequency synthesizer, the VCO gain is designed to be around 12MHz/V. Coarse frequency tuning is achieved by a 5-bit binary-weighted SCA at primary coil, while fine tuning is done by a varactor. Another SCA is also added at the secondary coil to achieve maximum tank impedance as discussed. MIM capacitors connected in series with the varactors decouple the varactors from high voltage swing, improve the Q factor and reduce the VCO gain at the expense of tuning range [16][17].

3.3.2 Sigma-Delta Modulator

a) Overview

Sigma-delta modulator (SDM) is widely used in fractional-N frequency synthesizer to suppress the fractional spurs. The SDM in a synthesizer is to randomize the instantaneous division ratio and perform noise shaping, hence push the quantization noise to higher frequency, and suppress it by the low pass loop filter. For frequency synthesis purpose, the SDM is quite different from those in data converters. Here,

SDM is a digital system; therefore it does not suffer from analog circuit imperfections such as electronic noise, finite gain-bandwidth, timing jitter, slew rate, and comparator hysteresis. Instead, the major considerations in the design of a digital noise shaper are: 1) order, which has to be decided according to the noise shaping requirement; Another important constraint is that the order should be equal or less than the order of loop filter to avoid an increased noise at intermediate offset frequency; 2) architecture, single-loop or MASH; 3) stable input range should be large enough to avoid any frequency dead band; 4) output levels; 5) noise transfer function (NTF); 6) bit width which determines the frequency resolution together with the reference frequency [18]. The above six key parameters are related to each other hence need to be examined collectively.

The ΣΔ quantization noise is modeled as an additive noise source at the prescalar output. The phase noise contribution of the ΣΔ modulator at the output of synthesizer is found as [7].

$$S_{\Sigma\Delta}(f) = \frac{\Delta^2}{12 \times f_{ref}} \times \frac{|H_{qz}(z)|^2}{|1 - z^{-1}|^2} \times |T(f)|^2 \tag{3-46}$$

where H_{qz} is the z-domain NTF of the ΣΔ modulator and *T(f)* is the PLL closed-loop transfer function $\frac{A_{open}(f)}{1 + A_{open}(f)}$.*Δ* is n×2π (minimum phase jump is n VCO period);

b) Comparison of digital SDM implementation

Digital SDM, unlike its analog counter parts, don't have any non-idealities. Therefore cascade modulators won't suffer from mismatches and noise leakage from front stages, and multi-bit quantizers won't suffer from any non-linearity. MASH

modulator is widely used because it provides the largest noise suppression for a give order, it is easy to implement in CMOS and unconditionally stable. However, single-loop modulator presents a better solution, showing less sensitivity to noise leakage and noise coupling and providing more flexibility [7]. Table 3.5 compares features of different modulator types.

Table 3.5 Comparison of digital modulators

Modulator type		NTF gain	Stable input range	Noise shaping	Output bit
Single-loop	Single output bit	Smallest	Smaller	Least noise shaping	Dual modulus divider, simple PLL architecture
	Multiple Output bit	Large	Larger	Desirable noise shaping, less tones	Multi-modulus divider, but less spread bit pattern
MASH (Cascade modulator)		largest	Absolute stable	Largest noise shaping for a given order	Wide spread bit pattern, stringent requirement on PFD and CP

c) SDM system design and modeling

Before modeling the SDM we should first and foremost design the noise transfer function of the modulator, which is of critical importance for successful implementation of the SDM and its stable operation.

The NTF can be designed using traditional Butterworth, Chebyshev or inverse Chebyshev functions. In this design, Matlab Delta-Sigma Toolbox “delsig” [19] is utilized to generate the noise transfer function of specified order and oversampling ratio. There are four types of SDMs in the toolbox. They are: CRFB (Cascade-of-resonators, feedback form); CRFF (Cascade-of-resonators, feedforward

form); CIFB (Cascade-of-integrators, feedback form); CIFF (Cascade-of-integrators, feedforward form).

The block diagram of the CIFB modulator is shown in Fig. 3.20. It is chosen because of the fact that delay elements Z^{-1} is inserted between every two serial adders, therefore breaks the series adder chain in the modulator and reduces the speed requirement of these digital adders.

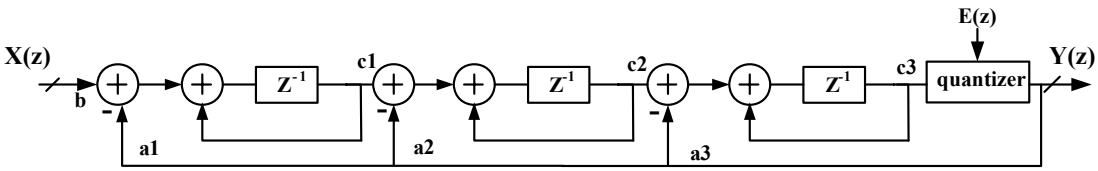


Fig. 3.20 Architecture of the CIFB modulator

The transfer function of the architecture shown in Fig. 3.20 can be derived as

$$Y(z)\{1+Az^{-1}+Bz^{-2}+Cz^{-3}\}=DX(z)z^{-3}+E(z)(1-z^{-1})^3 \qquad (3\text{-}47)$$

where X(z), Y(z) is the z-domain input and output signal, E(z) is the quantization noise. *A*, *B*, *C*, *D* are coefficients given as

$$\begin{aligned} A &: a_3c_3-3 \\ B &: c_2c_3a_2-2a_3c_3+3 \\ C &: c_1c_2c_3a_1-c_2c_3a_2+a_3c_3-1 \\ D &: c_1c_2c_3b \end{aligned} \qquad (3\text{-}48)$$

where *a,b,c* are scaling coefficients shown in Fig. 3.20.

In this work, Matlab Simulink is chosen for conducting high level simulation. Simulink is a software package for modeling, simulating, and analyzing dynamic systems. It supports linear and nonlinear systems, modeled in continuous time, sampled time, or a hybrid of the two. Because of the strong numerical power of Matlab and abundant models provided by Simulink, the time domain and frequency

domain analysis can be performed. Fig 3.21 shows the schematic of Simulink behavior simulation. Fig 3.22 compares the output bit pattern of MASH3 and proposed modulator, which shows that the latter has a much concentrated output bit pattern, which shows less sensitivity to noise leakage and coupling as well as PLL nonlinearities. Fig 3.23 illustrates the histogram of each stage's output. Since the SDM in synthesizer is to generate a fractional number, the X axis of the histogram should be within 1 for a stable modulator. By monitoring the histogram of each integrator output, the coefficient *a, b, c* are properly scaled to ensure optimized signal swing at the internal nodes of the modulator.

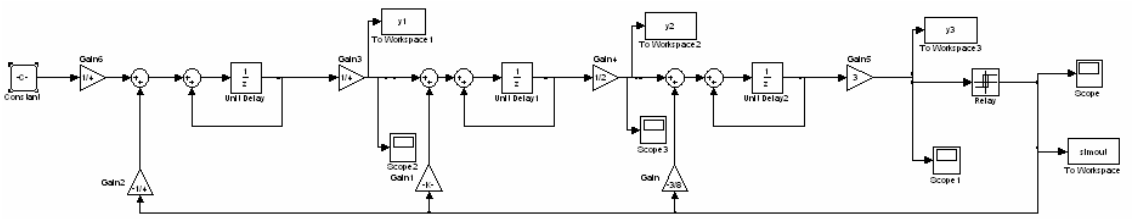
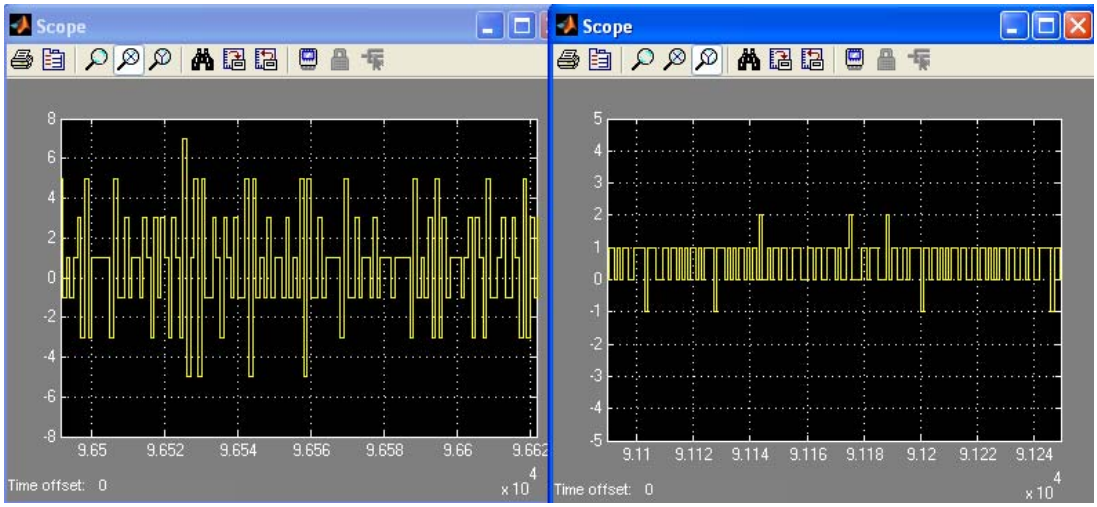


Fig. 3.21 Schematic of simulink simulation



(a) (b)

Fig. 3.22 Output bit pattern of (a) MASH3 (b) the proposed SDM

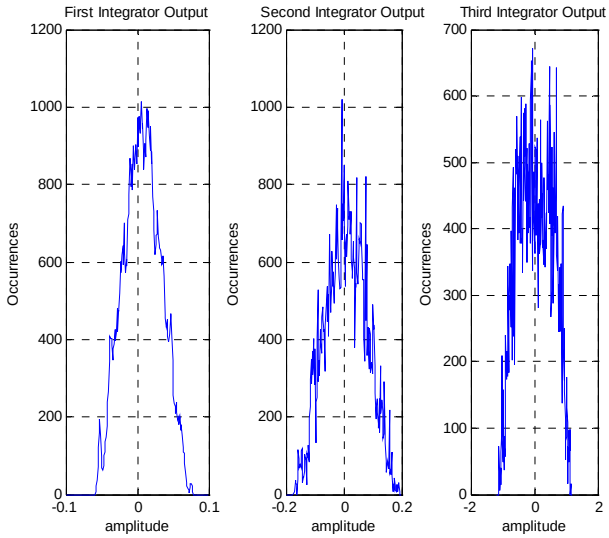


Fig. 3.23 Histogram of the modulator integrator output nodes

After intensive calculation and several iterations, an optimization in terms of phase noise, input stable range, and implement complexity is achieved. The final ΣΔ modulator is shown in Fig 3.24, while the coefficient is

$$\begin{aligned} a &= \{1/8;\ 1/4;\ \ (1/4+1/32)\} \\ b &= \{1/8\} \\ c &= \{1/2;\ (1/2+1/4);\ (4+2)\} \end{aligned} \tag{3-49}$$

Note that an additional constraint is that all coefficients are power of 2 so that expensive multiplier in digital logic can be avoided. Therefore, the final signal transfer function (STF) and NTF can be written as

$$NTF = \frac{Y(z)}{E(z)} = \frac{(1-z^{-1})^3}{1-1.3125z^{-1}+0.75z^{-2}-0.15625z^{-3}} \tag{3-50}$$

$$STF = \frac{Y(z)}{X(z)} = \frac{0.28125z^{-3}}{1-1.3125z^{-1}+0.75z^{-2}-0.15625z^{-3}} \tag{3-51}$$

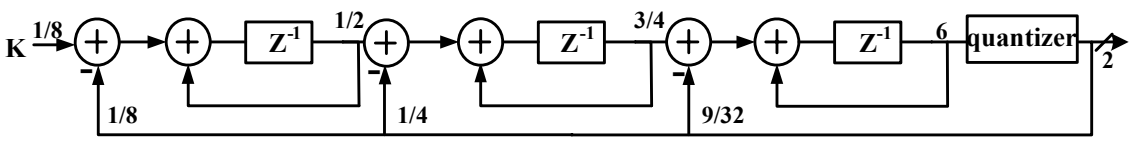


Fig. 3.24 Final single-loop ΣΔ modulator

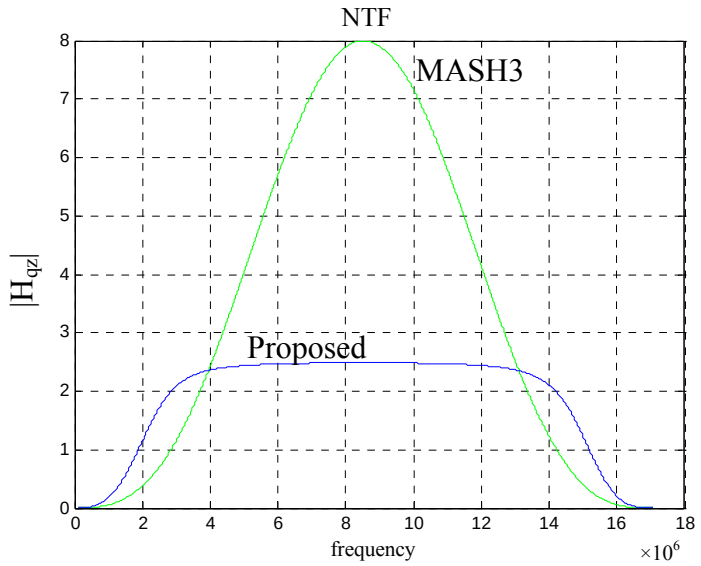
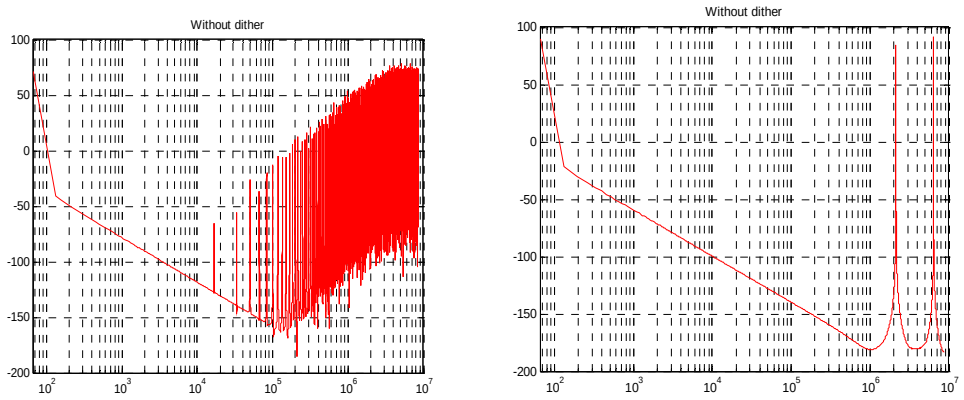


Fig. 3.25 NTF of the proposed ΣΔ modulator and MASH3

As can be seen in Fig 3.25, the proposed 3rd-order 2-bit SDM has a smaller noise at intermediate frequency compared with MASH3, since the latter push more noise to high frequency. The STF at DC are 1, therefore the signal is not attenuated.

d) Dither

For frequency synthesis purpose, the input to the ΣΔ modulator is DC value which stands for the fractional channel selection word, unlike in data converters. It is worth noting that DC inputs are the worst case inputs for a ΣΔ modulator, and thereby the output spectrum consists of pure tones and oscillations even when the order of the system is high. Fig. 3.26 depicts the output spectrum with DC input.



(a) (b)

Fig. 3.26 Output spectrum of ΣΔ modulator with DC input (a) 29/512 (b) 0.5

In order to randomize successive quantization errors samples and eliminate the spurious tones throughout the whole spectrum, dither is proposed in the literature to keep the input busy while applying a constant input to the modulator. The pseudo random signal is generated by maximal-length linear shift register sequences as shown in Fig. 3.27. To avoid an increase in the noise floor, it passes a 3rd-order highpass filter as shown in Fig. 3.28. Fig. 3.29 illustrated the output spectrum of the pseudo random signal with and without highpass filtering.

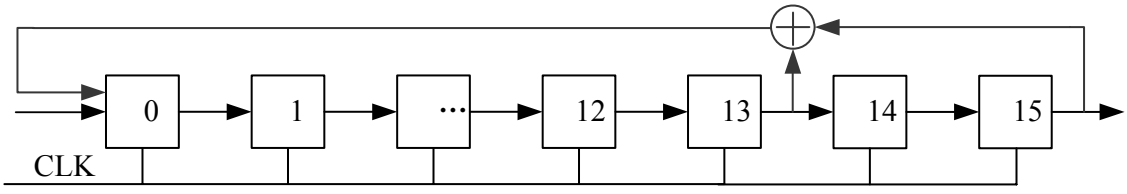


Fig. 3.27 Pseudo random sequence generator

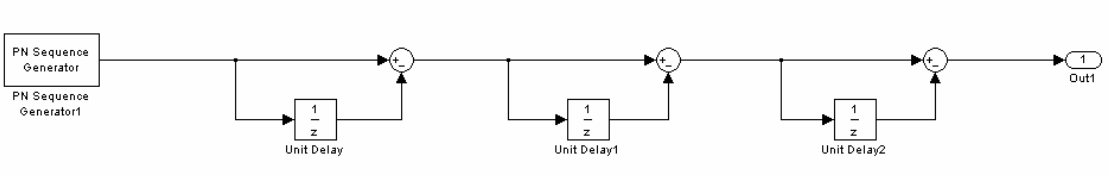


Fig. 3.28 Pseudo random sequence generator with 3rd-order highpass filter

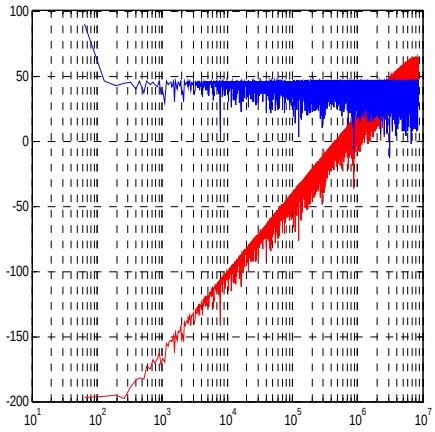


Fig. 3.29 Output spectrum of the pseudo random signal with and without highpass filtering

The complete modeling of ΣΔ modulator including dither in Simulink environment is shown in Fig. 3.30.

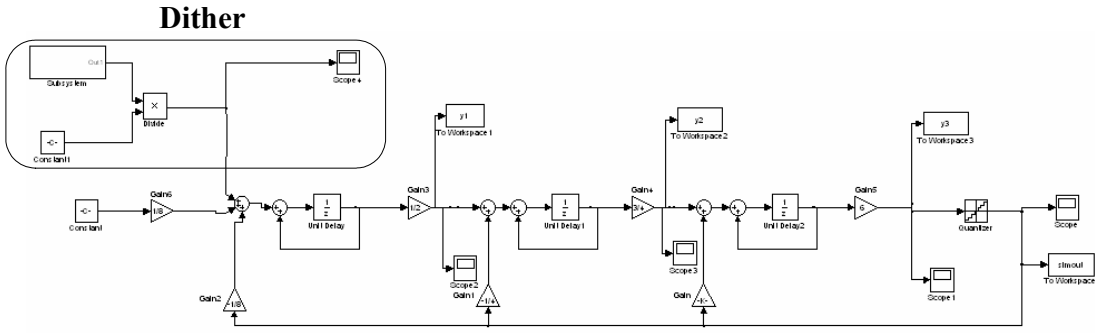


Fig. 3.30 Complete schematic of ΣΔ modulator in Simulink simulation

Output sequence of the ΣΔ modulator is stored to workspace, then Fast Fourier Transform (FFT) is calculated to obtain the frequency spectrum. In addition, the mean value of the output is calculated to compare with the expected fractional number. In this way, the functionality, stable input range, performance of the modulator can be checked in the behavior level.

e) Noise optimization

To achieve acceptable overall noise contribution of ΣΔ modulator, all the terms in

(3-46) have been carefully considered. As shown in Fig. 3.6, the programmable divider is connected after the second LO2 divider, so $\Delta=2\times2\pi$ in the proposed synthesizer since the ΣΔ quantization step size is two LO1 cycles. An alternative approach is to connect the programmable divider directly to the output of the first LO1 divider and to put the second LO2 divider outside the loop. By doing this, Δ in (3-46) is 2π, so the noise contribution of ΣΔ modulator is reduced by 6 dB. However, the programmable divider would have to operate at doubled frequency with wider programmable range, which would lead to significant power increase.

For the ΣΔ modulator H_{qz}, if the number of quantization levels is increased, the maximum passband gain of the NTF can be increased without causing any nonlinear stability problem. Although a 3-bit 8-level quantizer can provide larger passband gain compared with a 2-bit 4-level quantizer, the former expands the division ratios from {N, N+1} to {N–4, N+3} while the latter only requires {N–2, N+1}, which results in fewer output levels, less sensitivity to noise coupling and PLL nonlinearities, and reduced design complexity of the programmable divider.

f) Relationship between loop bandwidth and reference frequency for a target quantization noise

Since much of the energy of the ΣΔ quantization noise is shaped into high frequencies, we will assume that the quantization noise dominates at intermediate frequency range. For our target phase noise of -123dBc/Hz@1MHz, assume the quantization noise has to below -130dBc/Hz.

Assume the PLL has a simple butterworth transfer function with order *m* and a cutoff

frequency of f_o:

$$|T(f)|^2 = \frac{1}{1+(f/f_o)^{2m}} \tag{3-52}$$

It is chosen for the sake of simplicity in calculations.

Next, we assume the quantization noise dominates the output noise, i.e., all noise sources are set to zero except the ΣΔ quantization noise $L_{SD}(f)$. In the proposed synthesizer, L_{SD} can be expressed as

$$L_{SD} = \frac{(4\pi)^2}{12\times f_{ref}} \times \frac{|H_{qz}(z)|^2}{|1-z^{-1}|^2} \times |T(f)|^2 \tag{3-53}$$

In the following analysis, we will first investigate the MASH type modulator, and then compared with the proposed one.

For MASH architectures, $H_{qz}(z) = (1-z^{-1})^n$, where n is the order of MASH modulator. (3-53) can be rewritten as

$$L_{SD\_MASH} = \frac{(4\pi)^2}{12\times f_{ref}} \times \left(2\sin(\frac{\pi f}{f_{ref}})\right)^{2(n-1)} \times |T(f)|^2 \tag{3-54}$$

We can simplify the above expression by taking advantage of the assumption that f_{ref} is higher that the loop bandwidth, i.e.: $f_o \le f \le f_{ref}$, so that the following approximations can be made [20]

$$\sin(\frac{\pi f}{f_{ref}}) \approx \frac{\pi f}{f_{ref}} \tag{3-55}$$

$$|T(f)|^2 \approx (\frac{f_o}{f})^{2m} \tag{3-56}$$

Substituting (3-55) and (3-56), (3-54) then becomes

$$L_{SD\_MASH} = \frac{(4\pi)^2}{12\times f_{ref}} \frac{f_o}{f}^{2m} \left(\frac{2\pi f}{f_{ref}}\right)^{2(n-1)} \tag{3-57}$$

For convenience, the above equation is placed in a logarithmic scale that yields the units of dBc/Hz for the spectral density magnitude

$$10\log(L_{SD\_MASH}) = 10\log(\frac{4(2\pi)^{2n} f_o^{2m}}{12\times f_{ref}^{\,2n-1}}) - 20(m+1-\mathrm{n})\log(f) \tag{3-58}$$

(3-58) reveals that L_{SD} has a constant rolloff within the considered frequency range, of *-20(m+1-n)* dB/dec. The out-of-band phase noise dominated by VCO has a -20dB/dec rolloff, therefore to avoid increase in the noise due to the ΣΔ modulator, it is preferable to choose *m=n*. We will assume this constraint holds, so that the order of the loop filter is considered to be the same as that of the ΣΔ modulator. The last step is to determine the values of f_o that achieves the target noise requirements for different order of ΣΔ modulator and reference frequency f_{ref}. Rearrangement of (3-58) and substitution of *m=n* leads to the expression

$$f_{o\_MASH} = (\frac{L_{SD\_MASH}}{4})^{1/2m} \times f^{1/m} \times \frac{12^{1/2m}}{2\pi} \times f_{ref}^{\,(1-1/2m)} \tag{3-59}$$

Now, similarly, for the proposed 3rd-order ΣΔ modulator, the H_{qz} is given by (3-50). Follow the same procedure above mentioned, by making following approximation

$$\exp\left(\frac{2\pi if}{f_{ref}}\right) \approx 1+\frac{2\pi if}{f_{ref}}, \exp\left(\frac{4\pi if}{f_{ref}}\right) \approx 1+\frac{4\pi if}{f_{ref}}, \exp\left(\frac{6\pi if}{f_{ref}}\right) \approx 1+\frac{6\pi if}{f_{ref}} \tag{3-60}$$

Substitute (3-50), (3-56) and (3-60) into (3-53), after simplification, we obtain:

$$H_{qz}(z) = 2.5928\times 10^5 \frac{f_o^6 (f_{ref}^2 + 4\pi^2 f^2)}{f_{ref}^5 f^2 (f_{ref}^2 + 64\pi^2 f^2)} \tag{3-61}$$

Fig. 3.31 shows the maximum loop bandwidth versus reference frequency of MASH-2, MASH-3, MASH-4 and proposed ΣΔ modulator for the same target phase noise, i.e. *f=1MHz,* $H_{qz}=10^{-13}$.

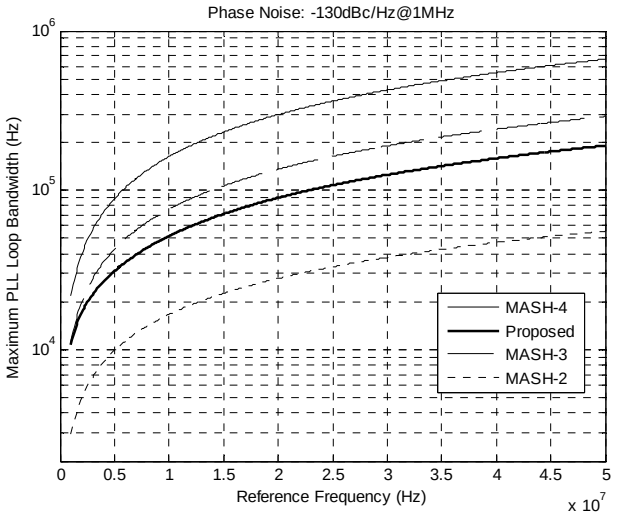


Fig. 3.31 Maximum loop bandwidth of MASH and proposed modulator to achieve the phase noise of -130dBc/Hz@1MHz

Thus, proper loop bandwidth can be selected to suppress quantization noise. Because the settling time requirement is quite relax (in the order of milliseconds), a narrow loop bandwidth of 35 kHz is chosen. Following the noise calculation introduced in 3.2.4 and as shown in Fig. 3.32, the out-of-band phase noise is always dominated by that of the VCO rather than that of the ΣΔ modulator. Therefore, optimization of the power consumption for a target phase noise is achieved at the architecture level of the proposed synthesizer.

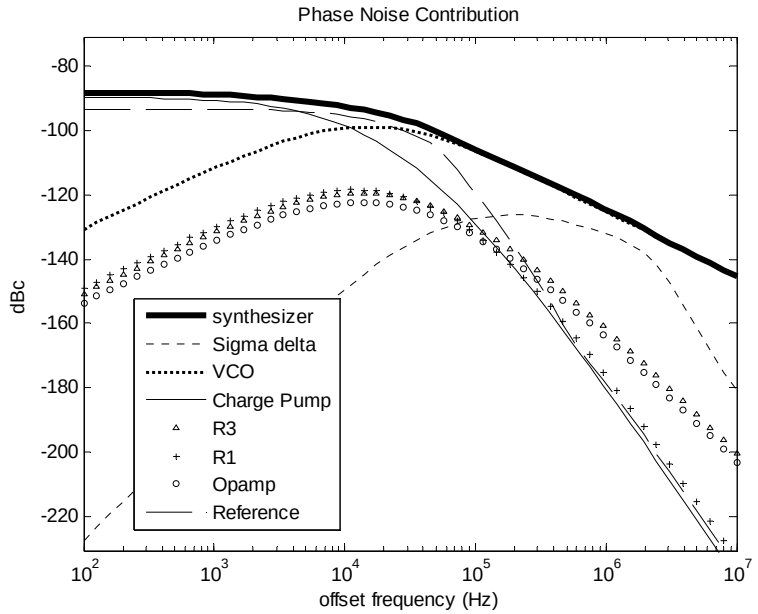


Fig. 3.32 Phase noise contribution in the proposed frequency synthesizer

g) RTL coding

The LO1 frequency in the proposed frequency synthesizer can be calculated as

$$f_{out} = 2 f_{ref} (N + \frac{K}{2^M}) \tag{3-62}$$

where f_{ref} is the reference input frequency, N is the integer channel selection part, K is input to ΣΔ modulator, M is the bit width of ΣΔ modulator. As can be seen from Fig. 3.6, to realize a RF channel spacing of 100 kHz, LO1 must be able to provide a frequency resolution of 2/3×100kHz. Therefore if f_{ref} is chosen as 51.2MHz divided by 3, M is calculated to be at least 9. The word-length of internal integrators in the ΣΔ modulator has to be long enough to avoid truncation errors. On the other hand, adder width should be limited to minimize power dissipation and area. The adder width needed is determined through exhaustive logic-level simulation of the modulator. Finally, 13-bit input and 16-bit internal adders have been chosen as an optimal solution.

Two's complement arithmetic is used to represent the digital signals throughout the proposed modulator. Not only can all the multiplier coefficients that are power of 2 be implemented using simple bit shifts, but also the quantization can be implemented as simple truncation of the 16-bit quantizer input to its 2 most significant bits [21]. Moreover, since the 16-bit representation of the 2-bit quantization signal Y(z) has the 14 LSB setting to 0. A change of sign, which in 2's complement logic, is inversion, followed by adding 1. As illustrated in Fig. 3.33, it can be simply implemented as a negation of the 2 MSB then followed by zeros.

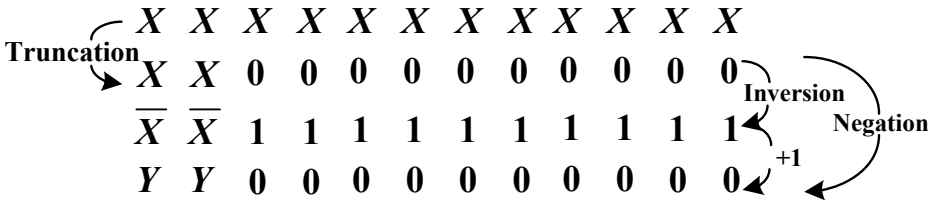


Fig. 3.33 Inversion and negation in 2's complement arithmetic

In 2's complement arithmetic, overflow of an adder results in a negative number. In a digital modulator, the effect of this overflow, or wrap-around, in the adders is equivalent to using hard limiters at the adder outputs, eliminating the overhead logic needed to implement hard limiters [22].

After RTL coding, the output bit pattern is stored and output spectrum is used to observe modulator performance. Average value of the modulator output is also calculated to compare with the expected one to prove the correctness of the modulator functionality. Simulation shows that the proposed modulator has a stable input range of around -0.9 to 0.25, which can satisfy the need of frequency synthesizer. Fig. 3.34 shows the simulated output spectrum after RTL coding. The

integer input is 100, corresponding to decimal number 18, the fractional part is 13'b0001000100101, corresponding to decimal number 549, so the actual input is 18+549/2048=18.26806640625. Simulation with 65536 No. of points generates a mean output of 18.26797894254978. The difference is only 8.746370021839311e-005=1.433LSB.

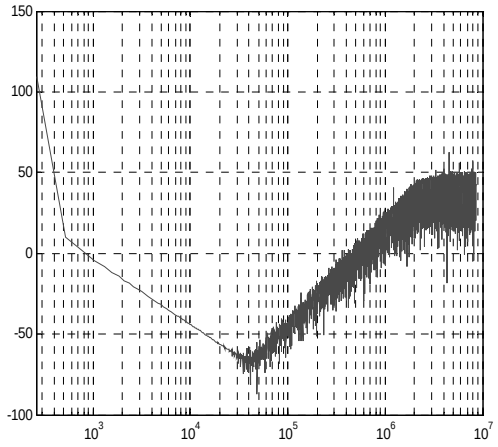


Fig. 3.34 Simulated output spectrum of the modulator after RTL coding

As shown in Fig. 3.34, the proposed ΣΔ modulator shows no spurious tones in the output. It can realize a frequency resolution of 25 kHz while dissipating only 0.12mW under 0.8V supply and 17MHz clock.

h) Design flow

The design flow of digital SDM involves quite a lot of tools. Start with Matlab Simulink behavior simulation, ModelSim for RTL level coding, DC_shell for auto-synthesis, Encounter for P&R, finally ModelSim together with library information and netlist after layout for post simulation. Meanwhile, schematic and layout can be generated in Cadence for DRC & LVS checking. Mixed-mode presim and postsim with analog part can be done in Cadence environment too. Fig.3.35

shows the complete design cycle of the mixed-mode circuit.

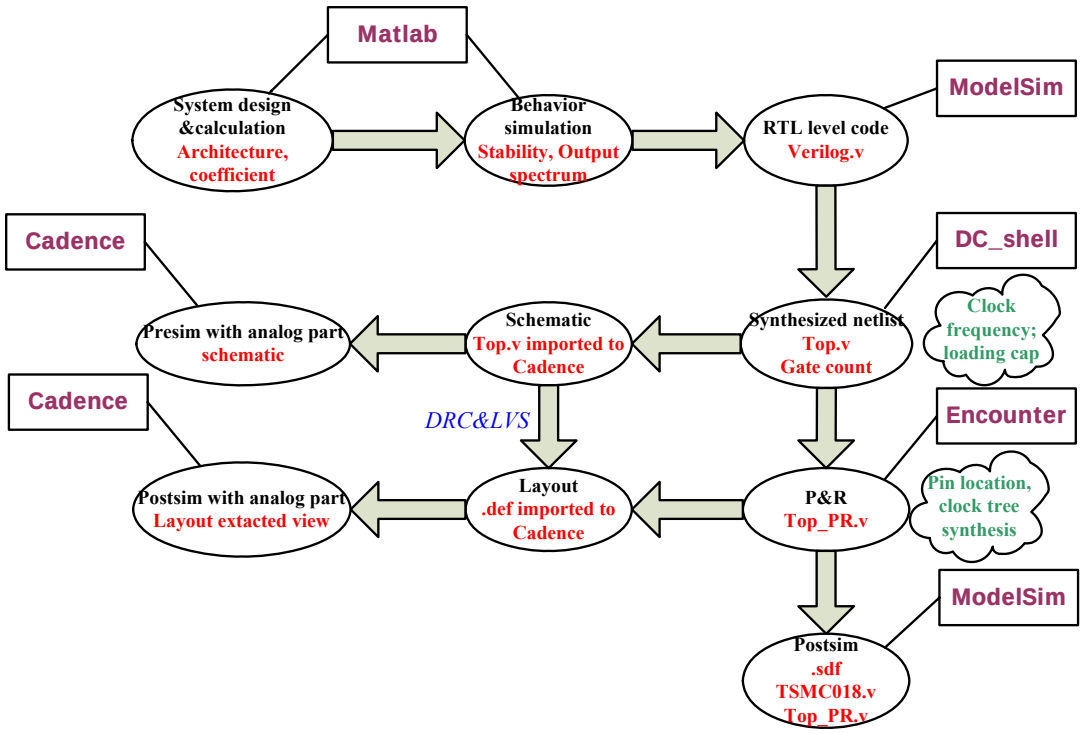


Fig. 3.35 Design flow of the digital SDM

3.3.3 Dividers

As shown in Fig. 3.6, several frequency dividers are required in the PLL loop. The high frequency SCL divider uses two D-latches in a master-slave configuration. Dynamic loading is utilized to achieve lower power consumption. AC coupling is employed to bias the PMOS loading transistor as well as current sources of the D-latches. Quadrature LO2I and LO2Q are available at the 2nd divider's outputs. Fig. 3.36 illustrates the schematic of the high frequency SCL divider.

Since the desired LO2 output frequency ranges from 860/3MHz to 320MHz, a variable division ratio of 16.796875 to 18.75 is required. Because the 2-bit output of ΣΔ modulator represents {–2, –1, 0, 1} and the ΣΔ modulator has a stable input range of {–0.9, 0.25}, the actual division ratio required is from 15 (17-2) to 20 (19+1). As

an example, for minimum division ratio of 16.8, the input channel selection word would be integer 17 and fractional –0.2, so the output of the modulator would be {15, 16, 17, 18}. Thus the minimum division ratio of the programmable divider is 15.

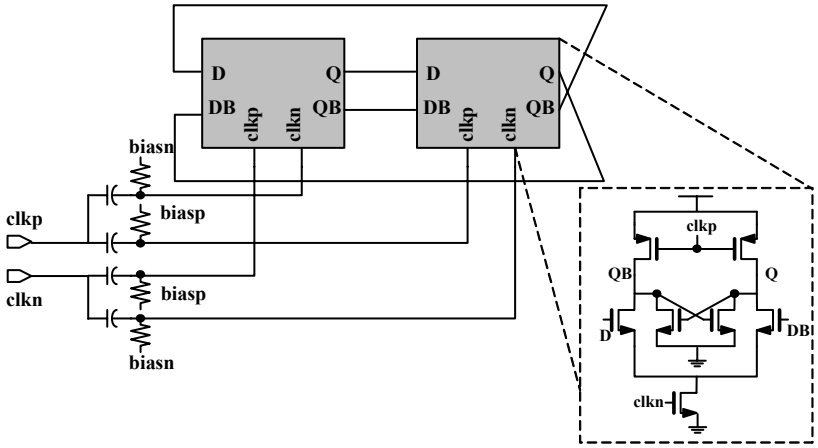


Fig. 3.36 SCL divide-by-2 schematic

A simple pulse swallow programmable divider shown in Fig. 3.37 is designed. Because of the small programmable range, only 3-bit swallow counter is needed, which requires three loadable D-flip-flops, while the program counter is a fix divide-by-7 circuits. The programmable divider operates at a relatively low frequency thus consumes only 480μW.

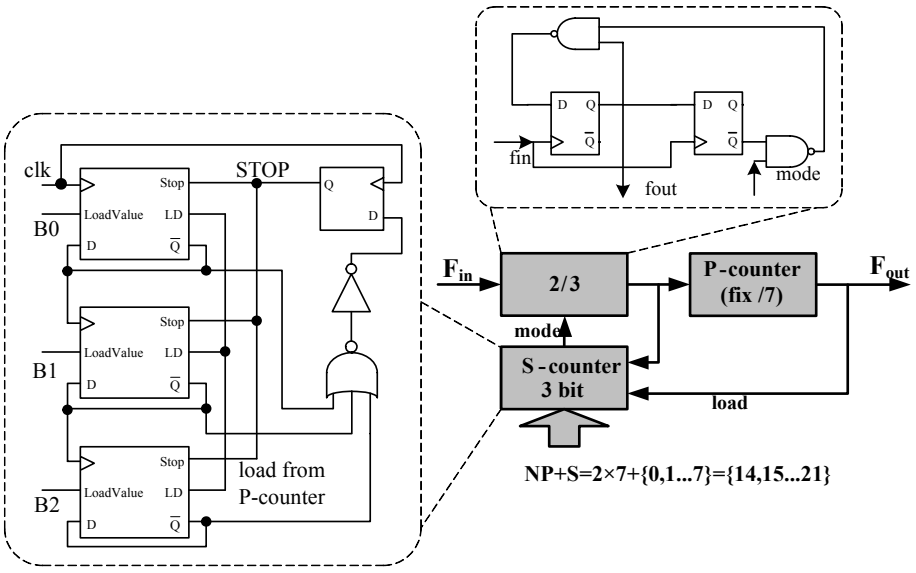


Fig. 3.37 Programmable divider

The key building block in the pulse swallow programmable divider is the loadable TSPC D-flip-flop. The conventional loadable TSPC D-flip-flop [5] shown in Fig. 3.38 is operated as follows. When the signal Stop is "1", Node n1 is discharged to "0" to isolate the input signal D and output signal $\overline{Q}$. Whenever LD="1", Node n2 and $\overline{Q}$ are made transparent to the LoadValue. When LD="0", Stop="0", and $\overline{Q}$=D, it functions as a divide-by-two, and the output only changes at the clock clk's rising edge. However, a problems occurs when LD="0", LoadValue="0" and clk="1". The output should be kept at "0" since the LoadValue "0" has just been loaded to $\overline{Q}$ and clk is high, so the output shouldn't change without a clock rising edge. But at this moment, Node n1 is in an unknown state. If the voltage at Node n1 happens to be higher than the threshold voltage V_{th}, Node n2 is discharged through M_{n2b} and M_{n2a}, which would cause a wrong output transition from "0" to "1". The situation is worse when the supply voltage is increased or the operation speed is low (after dividing down, the MSB in the S-counter has a clock speed close to the reference frequency), the output will be altered and cause malfunction. To solve the potential problem and provide robust performance, a selective path formed by M_{ps} and M_{ns} is added to make sure when LD="1" and LoadValue="0", Node n1 is pulled down to ground. Later when LD="0", Node n1 will remain to be low since the charge-up path is cut off by M_{p1b}. Therefore, the discharge of Node n2 is avoided to ensure correct function while other operations are not affected by this additional path. Fig. 3.38 shows the modified loadable TSPC D-flip-flop. Fig. 3.39 illustrates the simulation waveform before and after adding the selective path.

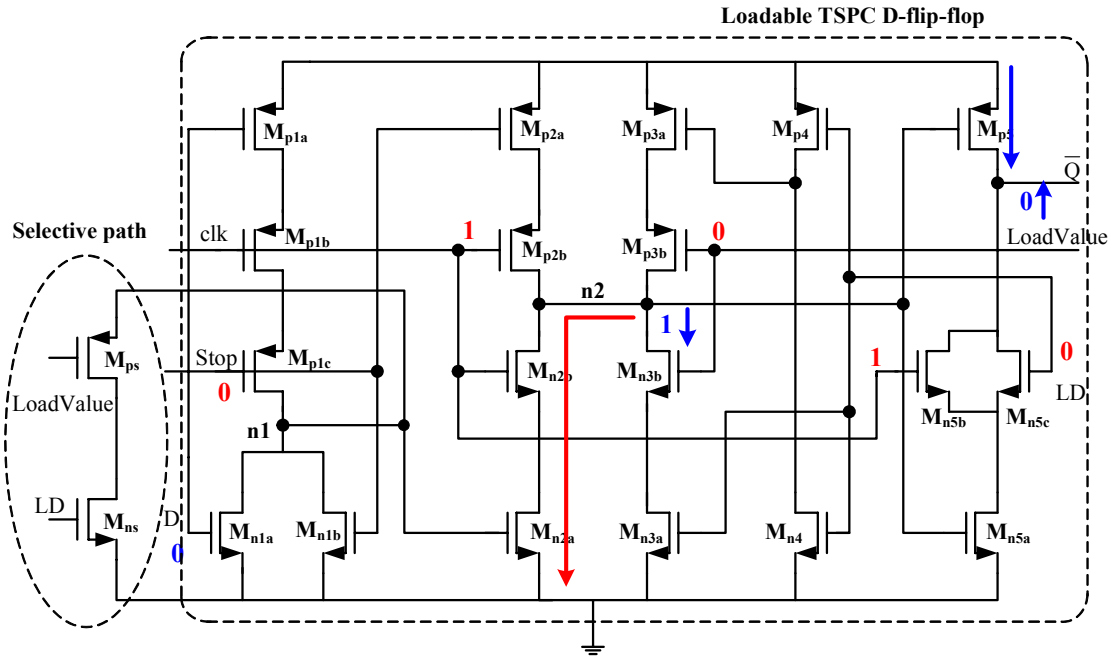


Fig. 3.38 Modified loadable TSPC D-flip-flop

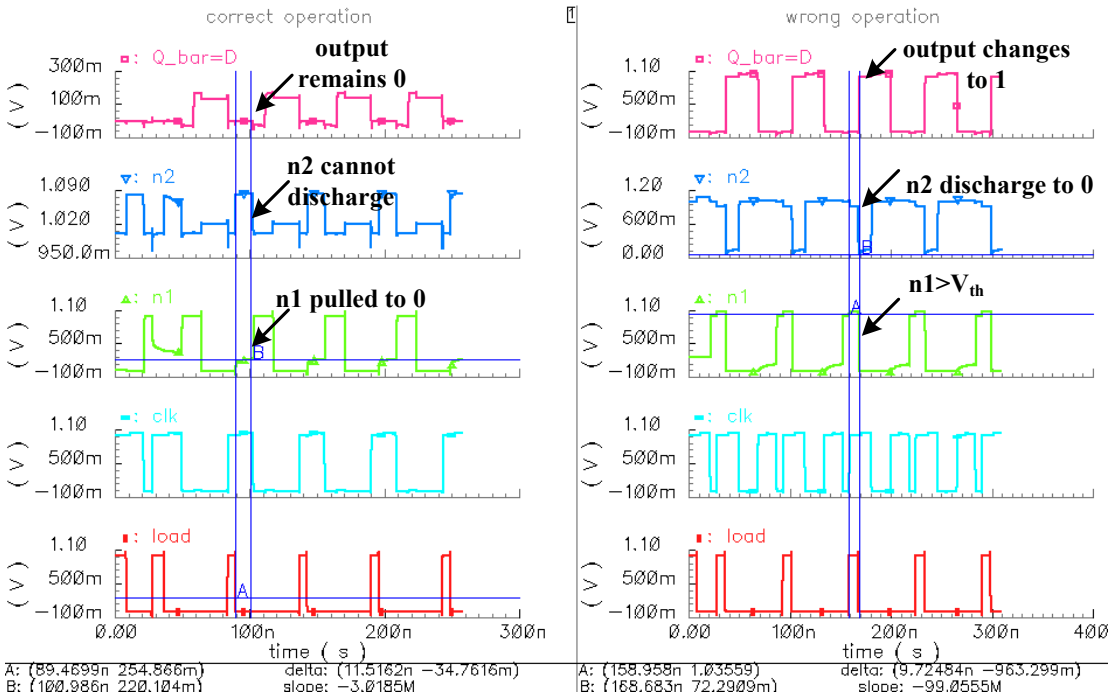


Fig. 3.39 TSPC D-flip-flop's operation after (left) and before (right) adding the selective path

3.3.4 Other Building Blocks

Conventional PFD and two charge pumps are implemented together with a third-order dual-path loop filter. The total capacitance in the loop filter is around

200pF. As the fractional spur is mainly caused by the current mismatch in the charge pump, layout is carefully optimized to provide good matching and to minimize the undesired coupling between digital and analog parts. Table 3.6 summarizes the component parameters used in the loop filter.

Table 3.6 Component parameters used in the loop filter

Component Parameter	Value
Loop bandwidth	35 kHz
I_{cp}	2μA
Charge pump current ratio B	30
R_1	14.7kΩ
C_1	60.1pF
C_2	48.1pF
R_3	9.81kΩ
C_3	90.2pF
K_{VCO}	12MHz/V

3.4 Experimental Results

3.4.1 Transformer Measurement

The transformer in the synthesizer is first designed by ASITIC. After a rough estimation of the inductance and dimension, the transformer is imported into Momentum from ADS for a more accurate simulation. The transformer layout with dimension indicated is shown in Fig. 3.40. Differential coils are used for both primary and secondary coils. The metal width is 15μm with a spacing of 1.5μm. A separate testing structure is put on chip for characterization of passive component.

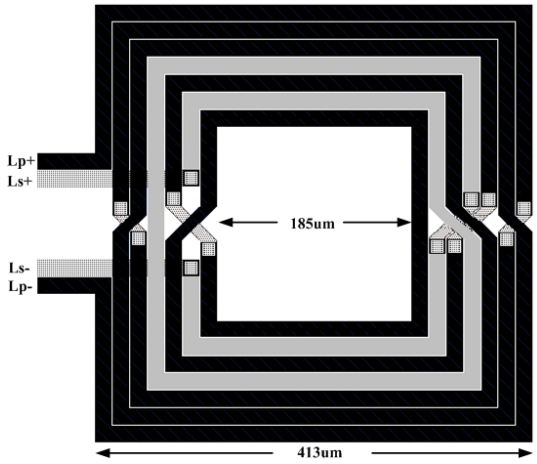


Fig. 3.40 Layout of the transformer

On-wafer testing structures are usually realized by placing the device under test (DUT) with one or two GSG pads, keeping interconnection lines as short as possible to allow probing with GSG RF probes [23]. Fig. 3.41 shows the testing structure of the transformer using two GSG pads. It can be seen that, apart from the signal-pad capacitance, the interconnections to the inductor will affect the measured impedances and hence accurate de-embedding will be required. Therefore, to characterize the parasitic capacitance and inductance from the GSG pad and interconnections one more testing structure with open and short configurations is implemented as shown in Fig. 3.42. Consequently, a two-step "open-short" de-embedding scheme [24] is applied to retrieve the pure S-parameter of the inductor.

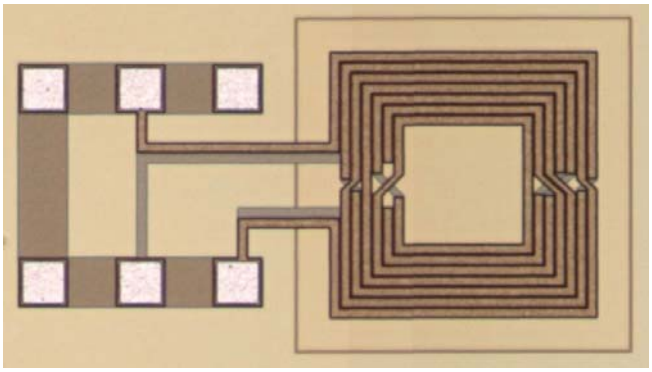


Fig. 3.41 Layout of the on-wafer transformer testing structure with two-port GSG

configuration

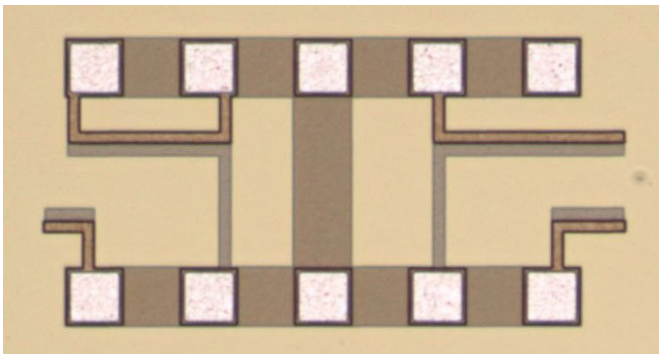


Fig. 3.42 Layout of structure for open and short calibration

In the two-step open-short de-embedding approach, it is assumed that all the parallel parasitics are located in the signal-pad and all the series parasitics in the interconnection lines. The corresponding equivalent circuit is depicted in Fig. 3.43.

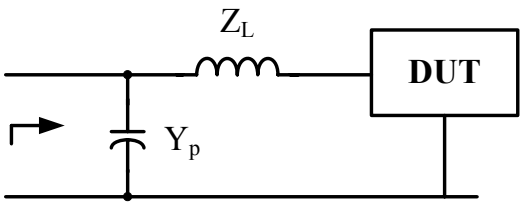


Fig. 3.43 Equivalent circuit model used for the two-step correction method

To enhance measuring accuracy, the two-port calibration with an impedance standard substrate is first performed. The parasitics surrounding the inductor is characterized by measuring the 'open' interconnection pattern and the 'short' pattern. Hence, the 'open' Y-parameter Y_{open} as well as a 'short' Y-parameter Y_{short} is obtained. The series impedances can now easily be found from the short measurement with some simple corrections from the open measurement, which is given by

$$Z_L=(Y_{short}-Y_{open})^{-1} \tag{3-63}$$

The actual Z-parameter of the inductor can be obtained

$$Z_{ind} = (Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \tag{3-64}$$

where Y_{DUT} is the measured Y-parameter matrix of the inductor together with all the parasitics.

First we need to measure S-parameter with network analyzer, then use ADS simulation to fit the S-parameter of the model into our measured S-parameter by selecting appropriate parameters of the elements in the model.

The model of the transformer is illustrated in Fig. 3.44. On top of the magnetic coupling factor of K between the primary coil (L_p) and the secondary coil (L_s) of the transformer, additional capacitive coupling C_p is included.

Table 3.7 summarizes simulated and measured results of the transformer. The measured parameter is quite close to the simulation. The inductance of the primary coil is 11nH with a Q of 4.36 at 1.2GHz, while the inductance of the secondary coil is 2.3nH with a Q of 2.6 at 1.2GHz. The coupling factor between the two coils is 0.684. Fig. 3.45(a) shows the simulated smith chart after model fitting. Fig. 3.45(b) shows the simulated quality factor of L_p and L_s after model fitting.

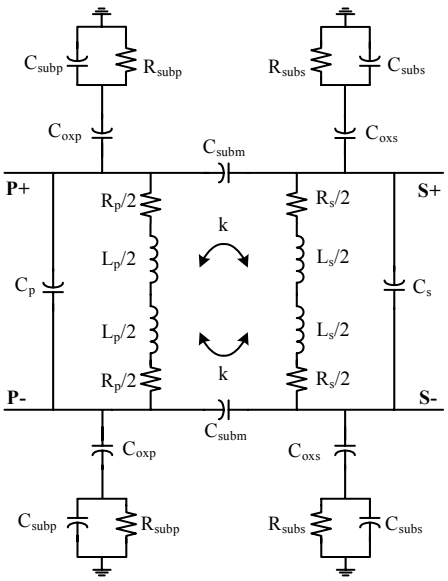
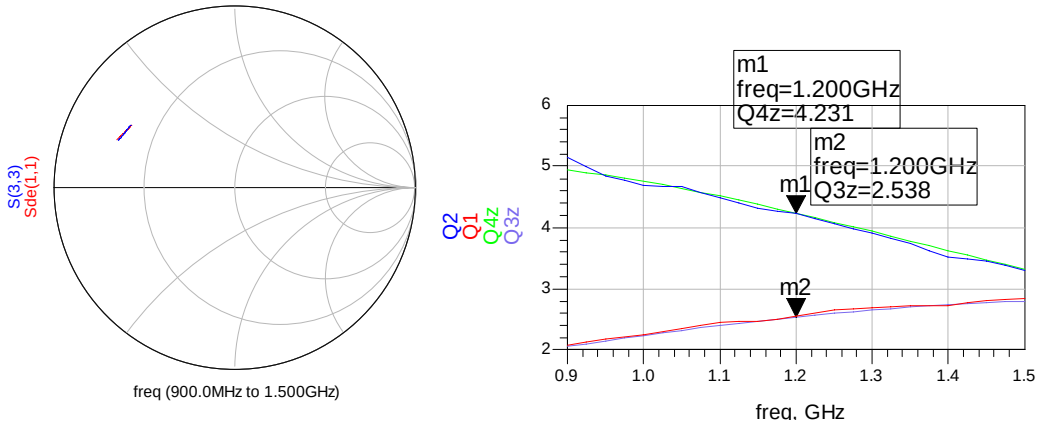


Fig. 3.44 Lump circuit model of the transformer

Table 3.7 Comparison of the simulated and measured results of the transformer

	L_p	Qp@1.2G	Ls	Qs@1.2G	K
Momentum	11.26	4.4	2.21	2.74	0.646
Sample1	10.06	4.23	2.299	2.54	0.685
Sample2	10.9	4.263	2.29	2.571	0.684
Sample3	11.036	4.36	2.292	2.6	0.685



(a) (b)

Fig. 3.45 Simulated transformer performance after model fitting (a) smith chart (b) quality factor

3.4.2 Frequency Synthesizer Measurement

The proposed frequency synthesizer is fabricated in 0.18μm CMOS process (V_{Tn}= 0.52V, V_{Tp}= –0.54V) with 6 metal layers. Fig. 3.46 shows the die micrograph of the proposed frequency synthesizer, which occupies a chip area of 1.65mm^2.

In Fig. 3.47, the frequency tuning characteristic of the proposed VCO is plotted versus the control voltage. At 0.8V supply, the VCO has a 31.8% tuning range from 1.038GHz to 1.43GHz. The tuning range is over-designed to make sure the desired frequency band can be covered even with the worst-case process variation. The VCO gain is about 18MHz/V at the upper frequency edge and about 8MHz/V at the lower frequency edge. The phase noise of the free running VCO is –122.5dBc/Hz at 1MHz

offset with a carrier frequency of 1.17GHz.

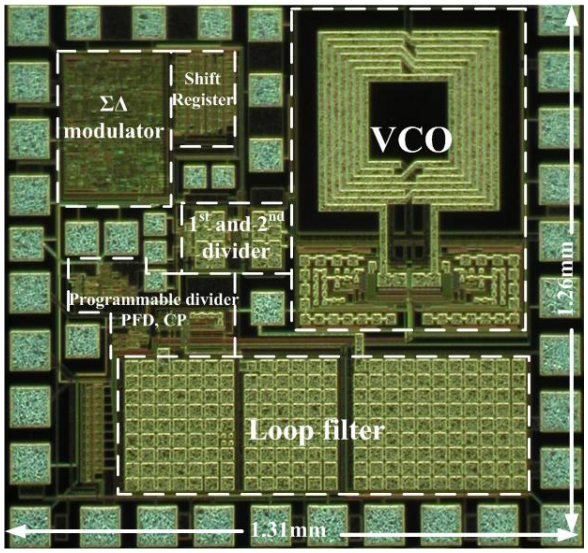


Fig. 3.46 Microphotograph of the proposed synthesizer

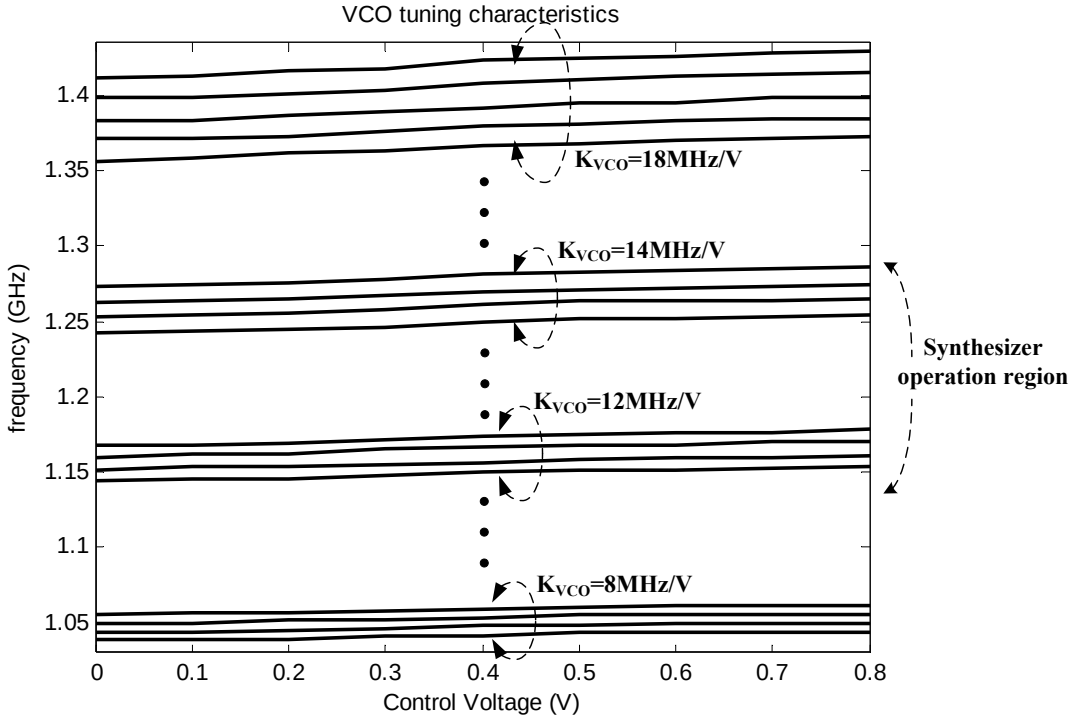


Fig. 3.47 Measured VCO frequency tuning characteristic

As illustrated in Fig. 3.48 the output spectrum of the synthesizer shows a reference spur of –84dBc at a center frequency of 1.17253GHz when operated with 0.8V supply. The phase noise of the synthesizer is measured by Agilent E4440A as shown in Fig. 3.49.

Phase noise at 200-kHz offset is –104dBc while at 1-MHz offset is –121dBc with a carrier frequency of 1.1725G and the fractional spurious tones are better than –70dBc. With the divide-by-two, the phase noise of the LO1 signals at 586.25MHz is –127dBc/Hz at 1MHz offset, which meets the system specification. The measured settling time for a frequency step of about 10MHz is 200μs, as shown in Fig. 3.50.

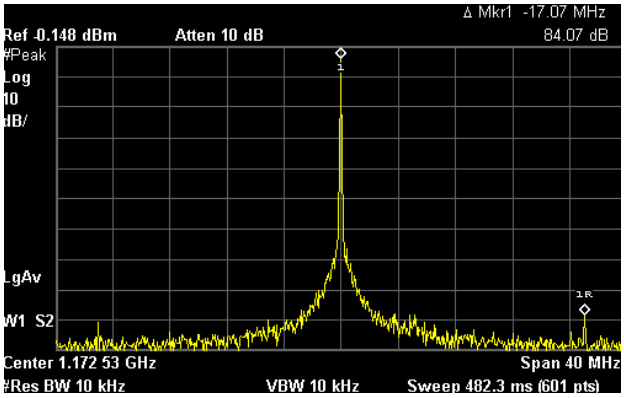


Fig. 3.48 Measured output spectrum of the proposed synthesizer

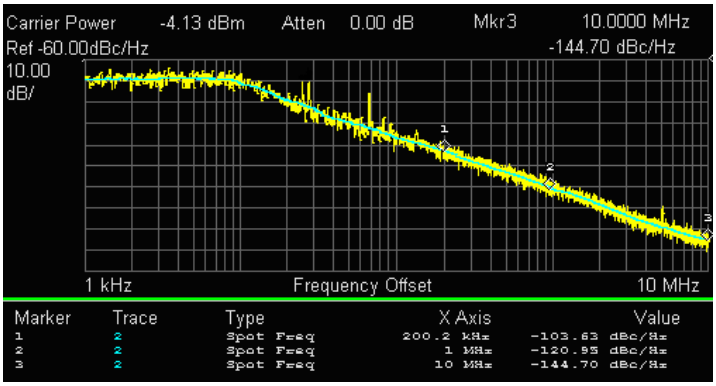


Fig. 3.49 Measured phase noise of the proposed synthesizer at 1.1725 GHz

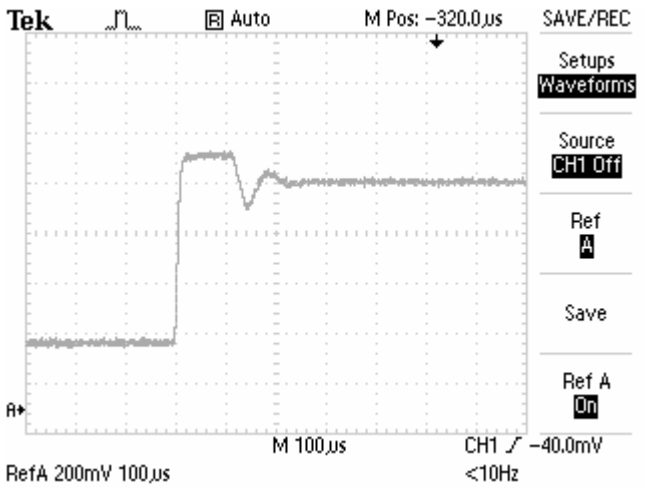


Fig. 3.50 Measured settling time of the synthesizer

At a supply voltage of 0.8V**,** the synthesizer consumes around 4.92mW, out of which 3.2mW is for the VCO, 0.12mW for the ΣΔ modulator, 1.36mW for all the digital dividers, and 0.24mW is for the opamp in the loop filter. The fractional-N frequency synthesizer can also operate at 1V, with the total power consumption of 7.4mW and the same phase noise performance as that of 0.8V, mainly due to the fact that VCO is operated in current limited region.

Table 3.8 summarizes the measured performance of the proposed frequency synthesizer together with that of recent state-of-the-art fractional-N synthesizers for comparison. The proposed synthesizer achieves comparable phase noise and spur performance while operating at the lowest supply voltage with the lowest power.

Table 3.8 Performance summary of fractional-N frequency synthesizers

Ref	[7]	[25]	[26]	[27]	This work
Supply voltage (V)	2	3.3	2.7	1.5	0.8
Process (µm)	0.25 CMOS	0.6 CMOS	0.35 CMOS	0.5 CMOS	0.18 CMOS
Output frequency(GHz)	1.8	1.675-1.795	1.48-1.88 0.86-1.09	0.84-0.97	1.06-1.4
ΣΔ modulator	3rd order,	MASH 2-1	3rd order	MASH-3	3rd order,

architecture	4 bit				2bit
Reference frequency (MHz)	26	20	19.68 or 19.2	25.6	17.1
Reference spur (dBc)	–75	N/A	N/A	–67	–84
Fractional spur (dBc)	<–100	<–70	–74	N/A	<–70
Phase noise (dBc/Hz@1M)	–124	–118	–134	–122	–121
Frequency resolution (Hz)	400	10	N/A	12.5k	25k
Chip area (mm^2)	4	10.73	4.4	0.99	1.65
Switching time (μs)	226	50	650	100	200
Power (mW)	70	52	37.8	30	4.92

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Chapter 4
RECEIVER ANALOG BASEBAND

4.1 Introduction

After RX front-end, RF signals are down-converted to baseband for further processing, including main signal amplification and interference rejection. Though operated at low frequency, baseband stage usually needs to provide substantial gain, while still preserve considerably good linearity. In addition, the proposed reader baseband is highly reconfigurable to deal with different system bandwidth and interference scenario for multi-protocol application. The baseband architecture consists of an active trap, an anti-aliasing filter with variable gain and a switched-capacitor channel selection filter with variable gain as shown in Fig. 4.1. The detailed design consideration, circuit implementation and experimental results are presented in this chapter.

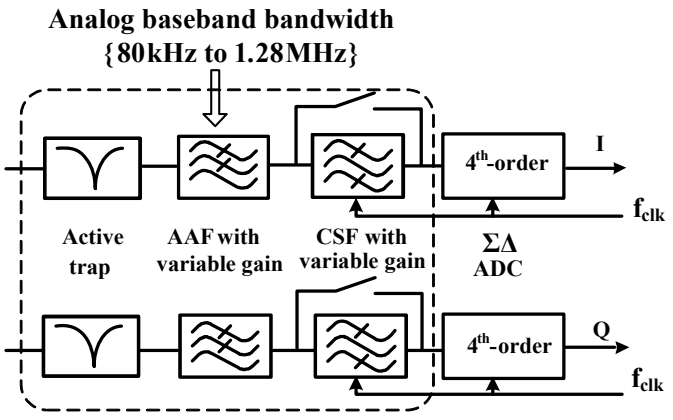
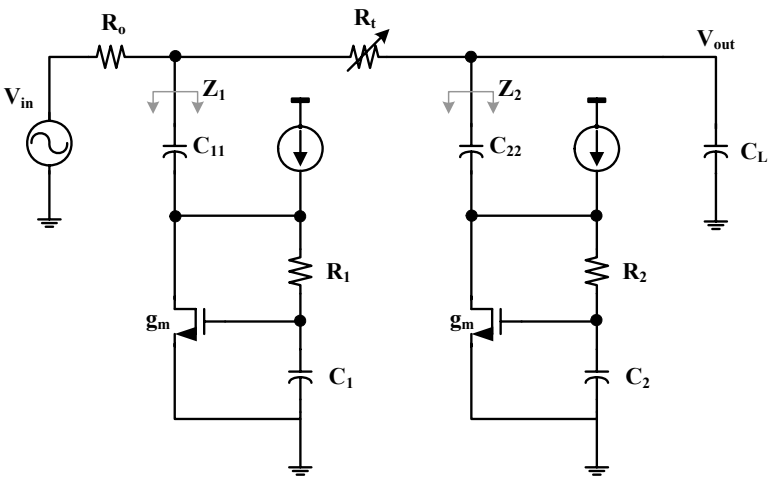


Fig. 4.1 Architecture of the receiver analog baseband

4.2 Tunable Active Trap

If AAF directly follows mixer, the linearity of AAF becomes the bottleneck in the receiver because of the amplification of signals and lack of filtering before it. An active-trap provides partial channel selection by synthesizing a notch at the adjacent or alternate adjacent frequency but keeping the signal band intact [1]. For the proposed multi-protocol reader, it has to furnish a tuning ability to reject interference at different offset frequency. The simple trap in [1] is modified so that two of them are coupled by a tunable resistor R_t as illustrated in Fig. 4.2. With proper biasing, transistor together with R_1 and C_1 presents inductive impedance in series with C_{11}, and thus generates a notch. In this work, C_{11} and C_{22} are chosen to be unequal, so the two traps are at slightly different frequency, therefore a wider notch can be obtained.



Component	value
R_o	1kΩ
C_{11}	60pF
R_1	40kΩ
C_1	18pF
g_m	~3mA/V
C_{22}	101pF
R_2	40kΩ
C_2	18pF
C_L	300fF
R_t	1k to 12kΩ

Fig. 4.2 Schematic of the tunable active trap and component value

The transfer function is calculated to be:

$$\frac{V_{out}}{V_{in}} = \frac{Z_1 Z_2}{sR_oR_tZ_2C_L + sZ_1Z_2R_oC_L + sZ_1Z_2R_tC_L + R_oR_t + R_oZ_1 + R_oZ_2 + Z_1R_t + Z_1Z_2} \quad (4\text{-}1)$$

where R_o is the output resistance of mixer. C_L is the loading capacitor from AAF, Z_1 and Z_2 are given as

$$Z_1 = \frac{1}{sC_{11}} // \frac{sR_1C_1 + 1}{g_m + sC_1} = \frac{s^2C_{11}R_1C_1 + s(C_{11} + C_1) + g_m}{s^2C_{11}C_1 + sC_{11}g_m} \quad (4\text{-}2)$$

$$Z_2 = \frac{1}{sC_{22}} // \frac{sR_2C_2 + 1}{g_m + sC_2} = \frac{s^2C_{22}R_2C_2 + s(C_{22} + C_2) + g_m}{s^2C_{22}C_2 + sC_{22}g_m} \quad (4\text{-}3)$$

Bias current, thus g_m and R_t, which is implemented by a 5-bit switched-resistor array, are tuned to generate notch at different frequency. The 3dB bandwidth is ensured to be larger than the signal bandwidth to keep the signal intact. Due to the low signal bandwidth, C_{11} and C_{22} are quite large. To minimize chip area, MOS cap is adopted. Fig. 4.3 shows the simulation results of the trap frequency tuning. 12dB attenuation improves the linearity of the receiver by 8dB at the cost of 1mW power consumption and chip area of 0.32mm^2.

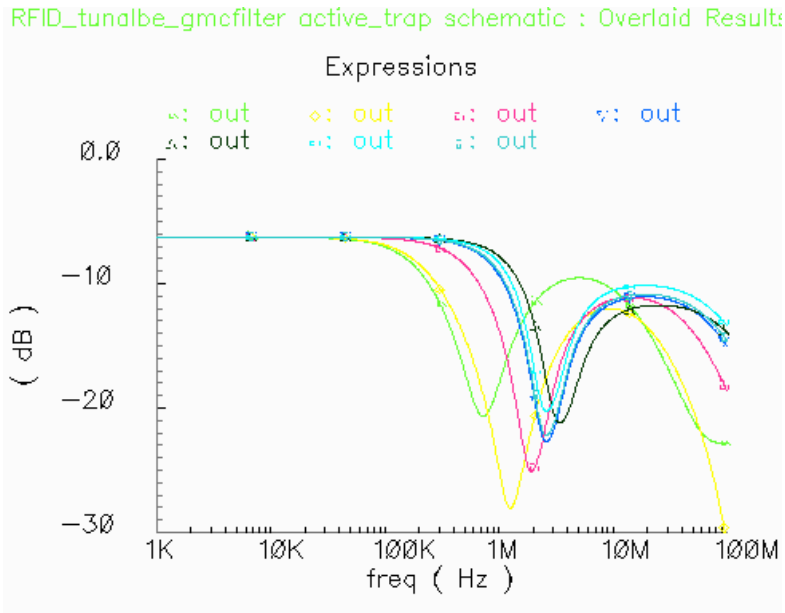


Fig. 4.3 Simulation results of the trap frequency tuning.

4.3 Receiver Anti-Aliasing Filter

4.3.1 Specification and Challenges

Due to a relative low system bandwidth, both CSF and ADC are switched-capacitor (SC) circuits for their accurate frequency response, large dynamic range and low

power potential. If switched-capacitor circuits are built at baseband, frequencies close to integer multiples of f_s will replicate into the baseband and will be indistinguishable from signal inputs. The replicated signals are said to be aliased. Therefore, an anti-aliasing filter has to be a continuous-time filter whose filtering requirements depend on the clock frequency of the sampled circuits. In this work, the system bandwidth is varied which can be accomplished by changing the clock frequency of the switched-capacitor filter and ADC, as a result, the challenge of the anti-aliasing filter is to be tuned over a sufficiently wide bandwidth so as to provide enough anti-aliasing for later SC circuits while still preserving a large dynamic range. The specification can be calculated as follows [2]:

1) For the largest BW of 1.28MHz, the OSR is 16 or 24, take 16 for example since it is the worst case for AAF, f_s=40.96MHz; target attenuation is the difference between the magnitude of the blocker at f_s and the minimum desired signal, added to the SNR_{out} of 11dB, that is, 90-35+11=66dB; assume 20dB/dec attenuation, $20 \bullet N \bullet \log \frac{f_s}{f_{BW}} > 66 \Rightarrow N_{\min} = 3$.

2) System BW is from 80 kHz to 1.28MHz. If we keep the same OSR of 16, f_s is 2.56MHz to 40.96MHz. That sets the tuning requirement of the AAF. For smallest bandwidth (80 kHz), target attenuation is 62dB at 2.56MHz, while for largest bandwidth (1.28MHz), target attenuation is 62dB at 40.96MHz.

3) Out-of-band IIP3 is 0dBV; Noise figure is 18dB; largest gain is 55dB with tunable range from 3dB to 58dB.

The challenges of the anti-aliasing filter are thus high linearity with tunable gain and

bandwidth. Due to the oversampling nature of the later stages, the requirement in bandwidth accuracy is greatly relaxed. The AAF is not expected to provide sharp rolloff on adjacent channel interference, so its bandwidth can be designed to be wider than signal bandwidth to tolerate process variations. As such, automatic tuning is not required for the AAF.

4.3.2 Passive Filter to Active Filter Conversion

There are two popular kinds of continuous time filter, namely active-RC filter and G_m-C filter. Fig. 4.4 shows a typical active RC integrator and its transfer function. Generally the resistors are implemented by triode region MOSFET for smaller chip area and tuning ability, so active-RC filter is also called MOSFET-C filter. Fig. 4.5 shows a schematic of the integrator formed by transconductor and capacitors, which is the basic building block in a G_m-C filter. MOSFET-C filter can be very linear because they are based on closed-loop opamps but the power consumption is considerable and the opamp needs to drive resistive load. In contrast, G_m-C filter operates in the open loop fashion thus provides a high speed low power potential but with worse linearity normally dominated by the g_m cells. Table 4.1 compares the features of the two kinds of continuous time filters. G_m-C filter is adopted in this work because of the low power feature.

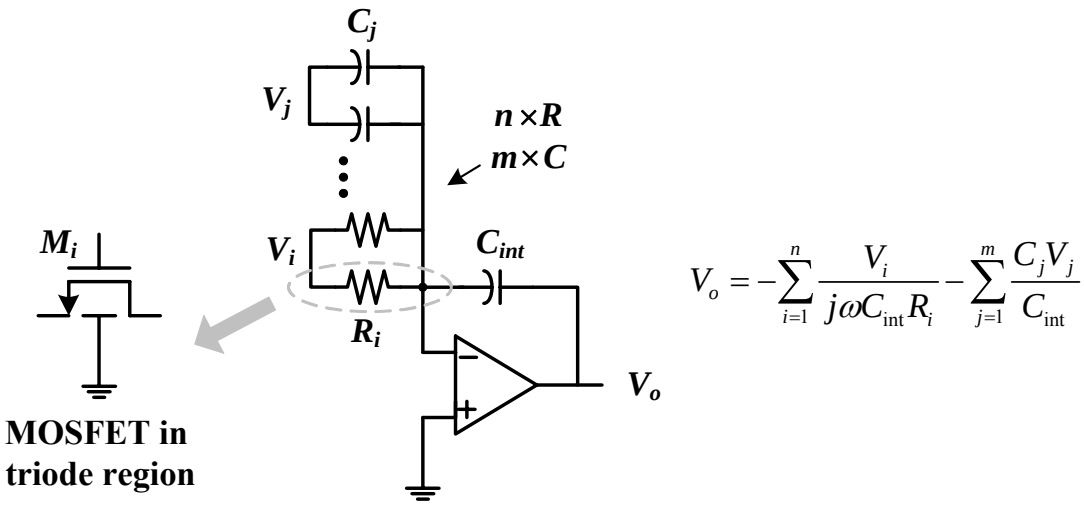


Fig. 4.4 Active RC (opamp RC) integrator

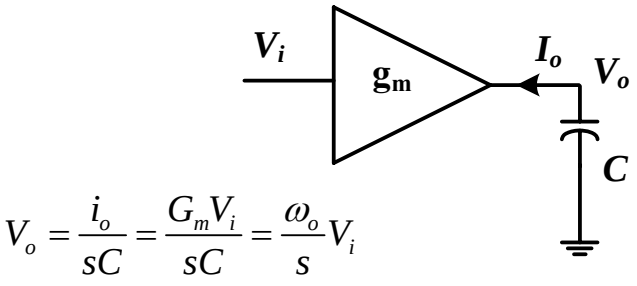


Fig. 4.5 Transconductor and capacitor Integrator

Table 4.1 Features of Active-RC filter and G_m-C filter

	Active-RC filter	G_m-C filter
Pros	Feedback reduces sensitivity to parasitics	Based on simple open-loop OTAs
	Small area and low power for frequency< ~100kHz	Small area and low power for frequency < ~100MHz
	Moderate-to-high precision with tuning	Moderate precision with tuning
Cons	Opamp and feedback limit use of bandwidth	Sensitive to parasitics
	Not suited for high frequency applications	Worse linearity and dynamic range
	On-chip tuning and corresponding circuitry	On-chip tuning and corresponding circuitry

As can be seen from table 4.1, both two kinds of filters need on-chip tuning, primarily due to the difficulties to realize accurate value of resistor, capacitors, g_m and to match them well. This inevitably causes the deviation of filter's transfer

function from its designed value. To reduce the sensitivity to parasitics, continuous time filters are normally synthesized by the doubly terminated RLC filter to maintain its low sensitivity to component variations [3]. There are mainly three ways to perform the passive to active conversion.

a) Signal Flow Graph

In this approach, we first write down state equations, then draw the signal flow graph for each state, after combining all the sub-graph, we can obtain the final signal flow graph to synthesis the whole filter. A 3rd-order elliptic low-pass ladder filter is illustrated in Fig. 4.6 as an example.

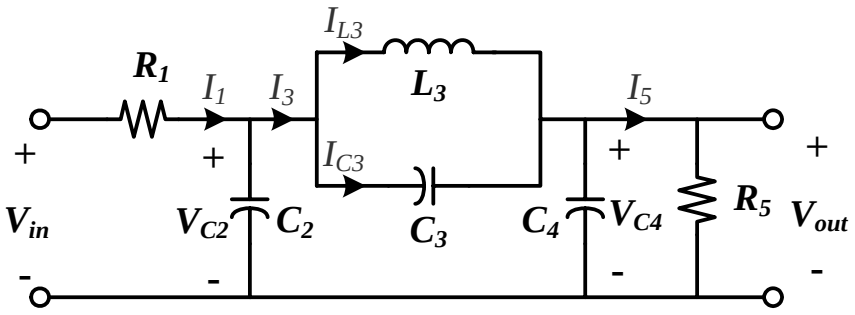


Fig. 4.6 Schematic of a 3rd-order elliptic low-pass filter

First, write down the state equation for V_{C2}

$$sC_2V_{C2} + I_{L3} + I_{C3} = I_1 \tag{4-4}$$

Where I_1 and I_{C3} can be written as

$$I_{C3} = sC_3(V_{C2} - V_{C4}) \tag{4-5}$$

$$I_1 = \frac{V_{in} - V_{C2}}{R_1} \tag{4-6}$$

Substituting (4-5), (4-6) into (4-4) results in

$$V_{C2} + \frac{V_{C2}}{s(C_2 + C_3)R_1} = \frac{C_3V_{C4}}{C_2 + C_3} + \frac{V_{in}}{sR_1(C_1 + C_3)} - \frac{I_{L3}}{s(C_2 + C_3)} \tag{4-7}$$

The signal flow graph of state V_{C2} is shown in Fig. 4.7.

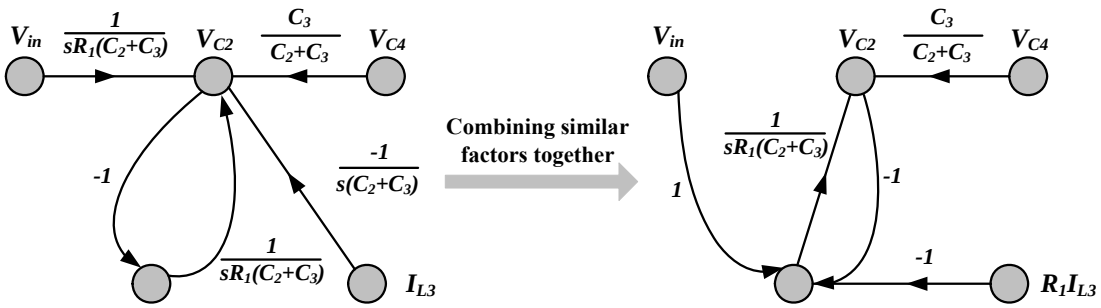


Fig. 4.7 Signal flow graph of state V_{C2}

Similarly for state V_{C4}

$$sC_4V_{C4} + \frac{V_{out}}{R_5} = I_{L3} + sC_3(V_{C2} - V_{C4}) \tag{4-8}$$

Rearranging (4-8), we have

$$V_{C4} = \frac{-V_{out}}{sR_5(C_3 + C_4)} + \frac{I_{L3}}{s(C_3 + C_4)} + \frac{C_3V_{C2}}{C_3 + C_4} \tag{4-9}$$

Thus signal flow graph of state V_{C4} can be drawn in Fig 4.8.

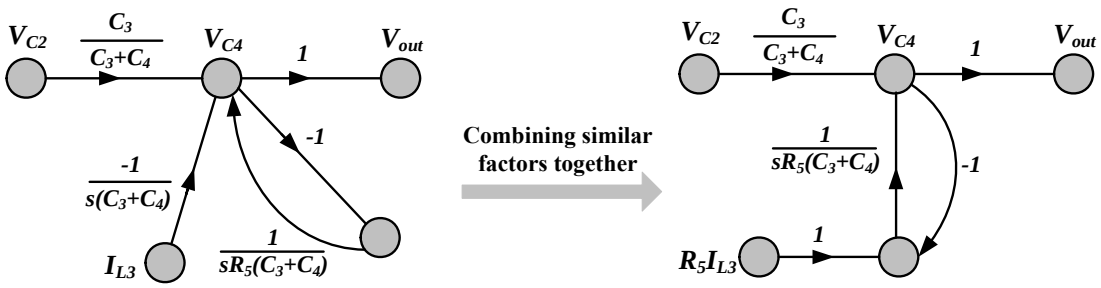


Fig. 4.8 Signal flow graph of state V_{C4}

Finally, state I_{L3} are analyzed

$$I_{L3} = \frac{V_{C2} - V_{C4}}{sL_3} \tag{4-10}$$

The signal flow graph of state I_{L3} is shown in Fig 4.9.

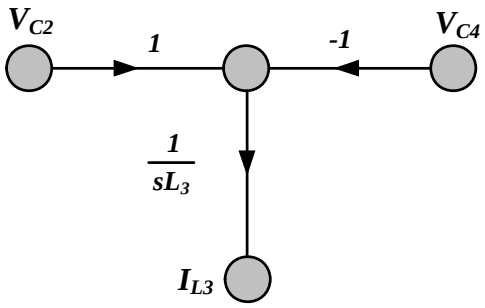


Fig. 4.9 Signal flow graph of state I_{L3}

Combining the three sub-graph, we obtain the final signal flow graph as depicted in Fig. 4.10. To synthesize the active G_m-C filter, the rules are

1) The "1" branch is g_m.

2) All transconductances are $1/R_1$.

3) 1/s branch is capacitor to ground.

4) Gains $C_3/(C_2+C_3)$ and $C_3/(C_3+C_4)$ can be realized by capacitor ladder as shown in Fig. 4.11.

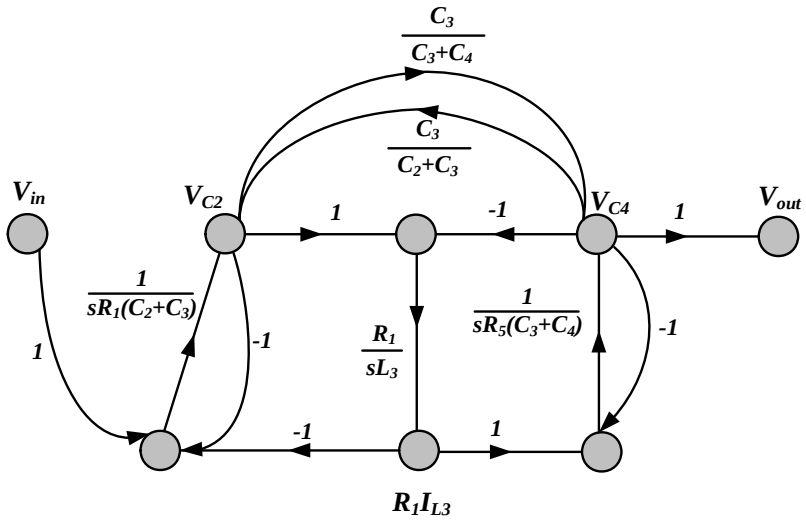


Fig. 4.10 Final signal flow graph

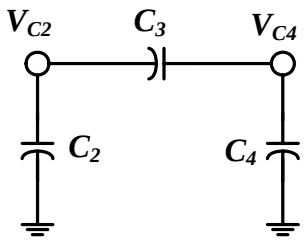


Fig. 4.11 Implementation of gain by capacitive ladder

The synthesized active G_m-C filter is shown in Fig. 4.12.

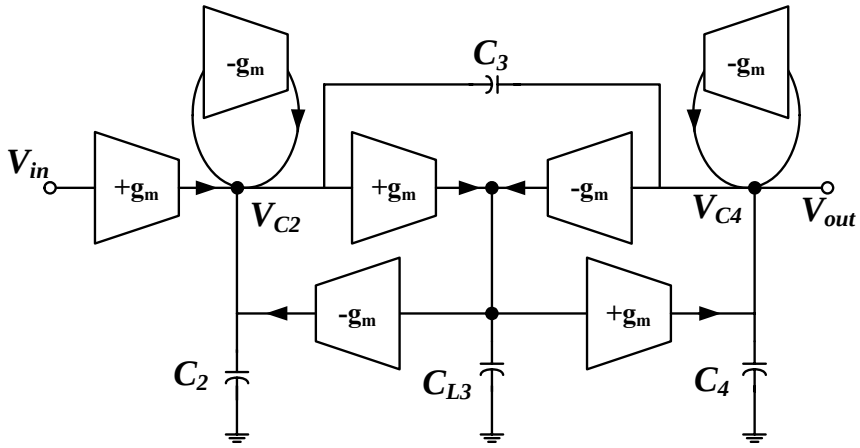


Fig. 4.12 G_m-C filter synthesized from passive ladder filter

b) Gyrator Method

Gyrator method is an element replacement approach. In a G_m-C filter, all the inductors and resistors are synthesized by g_m cells and capacitors. We will first derive the basic representation of active inductors and resistors, starting from single-ended to differential. The gyrator design flow is exemplified by a 3rd-order low-pass elliptic filter. A grounded inductor can be generated as shown in Fig. 4.13.

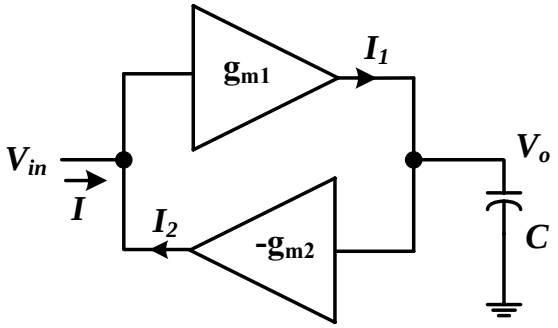


Fig. 4.13 Grounded inductor generated by gyrator

The impedance looking into the input can be calculated by writing down the following I-V equations

$$I_1 = V_{in} g_m \tag{4-11}$$

$$I_2 = -V_o g_m \tag{4-12}$$

$$I = -I_2 = V_o g_m \tag{4-13}$$

$$V_o = \frac{I_1}{sC} \tag{4-14}$$

Calculating (4-11) to (4-14), we obtain the equivalent impedance

$$Z = \frac{V}{I} = \frac{SC}{g_{m1} g_{m2}} \tag{4-15}$$

It is seen that the circuit shows an inductive behavior. So the capacitance has been gyrated into an inductance. Similarly a floating inductor can be synthesized by the circuit shown in Fig. 4.14.

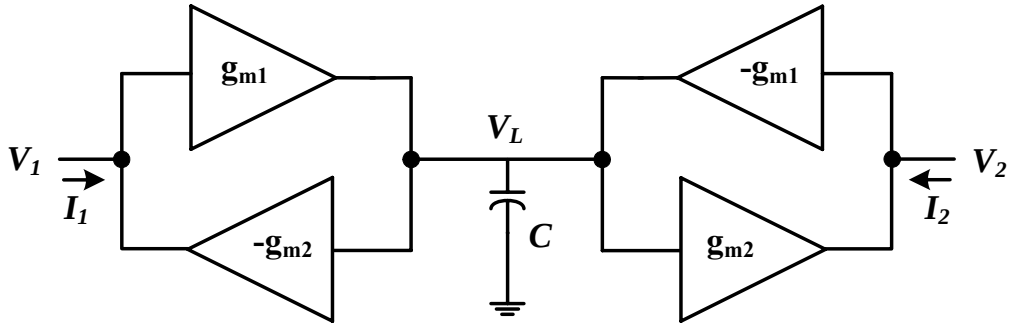


Fig. 4.14 Floating inductor generated by gyrator

We can write the equation at node V_L based on the Kirchhoff Current Law.

$$sC_L V_L + g_{m1} V_1 - g_{m1} V_2 = 0 \tag{4-16}$$

Therefore, voltage at node V_L is

$$V_L = \frac{g_{m1}(V_2 - V_1)}{sC_L} \tag{4-17}$$

Current I_1 and I_2 are expressed as

$$I_1 = -g_{m2}V_L = -g_{m2}\frac{g_{m1}(V_2 - V_1)}{sC_L} \tag{4-18}$$

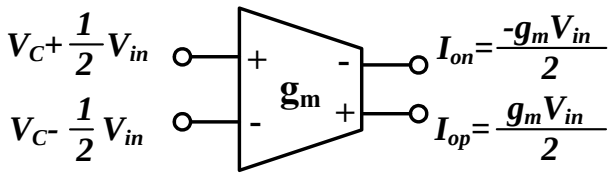
$$I_2 = g_{m2}V_L = g_{m2}\frac{g_{m1}(V_2 - V_1)}{sC_L} = -I_1 \tag{4-19}$$

The impedance can be calculated and simplified by making use of (4-17) to (4-19)

$$L = \frac{V_1 - V_2}{I_1} = \frac{sC_L}{g_{m1}g_{m2}} \tag{4-20}$$

By choosing proper value of C_L, g_{m1} and g_{m2}, desired value of floating inductance can be attained.

For high frequency operation usually balanced operation is preferred because of its immunity to the even harmonics, common mode noise and crosstalks. Besides, symmetrical transconductors have superior linearity and dynamic range over their single-ended counterpart. In addition, signal inversion is easy to implement in differential circuits. A differential transconductor is depicted in Fig. 4.15.



$$I_{out,diff} = I_{op} - I_{on} = g_m V_{in} = g_m V_{inp-} V_{inn}$$

Fig. 4.15 A differential transconductor

Using balanced transconductor, the floating inductor in Fig. 4.14 is redrawn in Fig. 4.16. The effective inductance is

$$L = \frac{V}{I} = \frac{C_L}{g_m^{\ 2}} \tag{4-21}$$

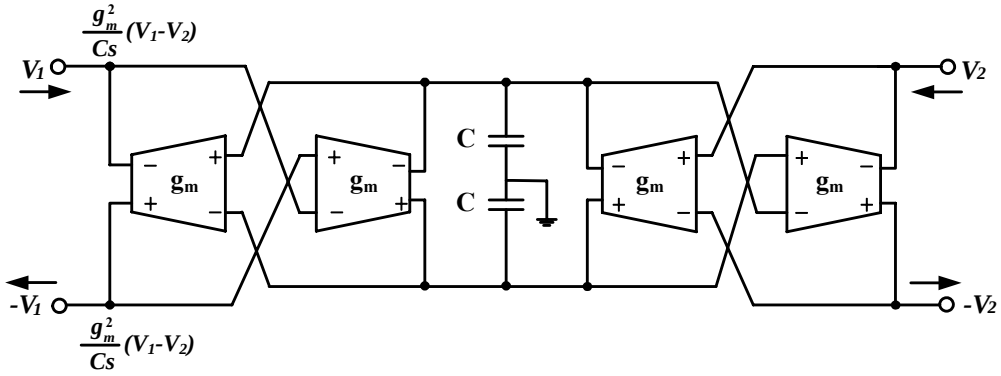


Fig. 4.16 Symmetrical floating inductor

We have illustrated how the grounded and floating inductors are replaced by g_m cells and C. As mentioned before, in a G_m-C filter, not only the inductors but also the resistors are to be replaced by g_m and capacitors. A resistor can be implemented in a feedback fashion as shown in Fig 4.17. Note that the circuit generates two grounded resistors of value

$$R = \frac{V}{I} = \frac{V}{g_m V} = \frac{1}{g_m} \tag{4-22}$$

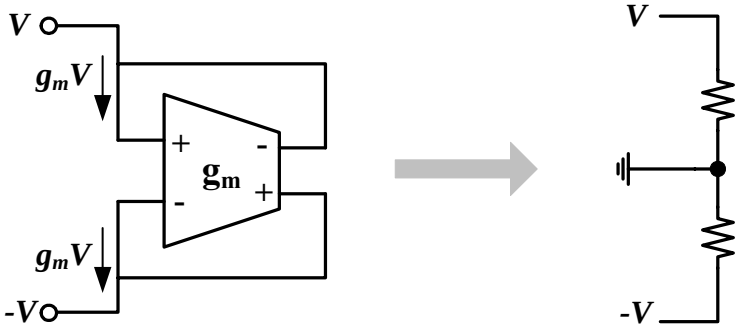


Fig. 4.17 Resistors generated by G_m cells

Therefore, by using Fig. 4.16 and Fig. 4.17, all the resistors and inductors in a passive ladder filter can be replaced by g_m cells and capacitors. Compared with signal flow graph, gyrator method has a better modularity, therefore eases the design, though the two conversion methods lead to the identical circuit. As an example, Fig.

4.18 shows the schematic of a balanced G_m-C filter converted from the 3rd-order elliptic low pass filter using element replacement approach.

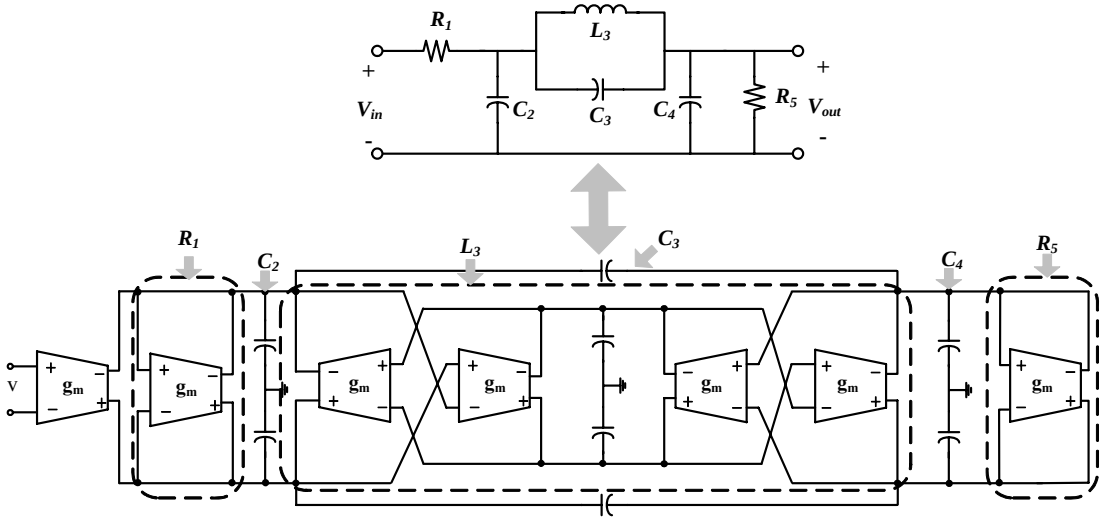


Fig. 4.18 A G_m-C filter converted from passive ladder using gyrator method

Note that we implement the source and load resistor as $R=1/g_m$ instead of a real resistor. By doing this, the g_m will appear as a frequency scaling factor. The transfer function just shifts along the frequency axis with no change in magnitude or phase performance. Small increase in peaking at the passband corner and the reduced notch depth for increased g_m case are caused by the small phase error of the transconductance that has a larger effect at higher frequencies. If we implement the resistor by a real resistor, serious deviation in transfer function behavior is visible, because the changed denominator coefficients of the filter transfer function are critical. They result in large peaking at the passband corner, reflecting an increased Q. This distortion is very difficult to correct since it is not obvious which component should be varied to bring about the needed change. It becomes clear that simulating resistors as $1/g_m$ is highly advisable in G_m-C filters [3].

c) Cascading Biquads

If we don't start the active filter from passive ladder, another way is to cascading several stages of biquads. Biquad filters can realize a general filter transfer function of second order. Its transfer function is given as

$$H(s) = K\frac{a_2 s^2 + a_1 s + a_0}{s^2 + s\frac{\omega_0}{Q_p} + \omega_0} \tag{4-23}$$

Depending on the choice of coefficients, a generic biquad can realize high-pass, low-pass, band-pass or band-stop characteristics. For example, $a_2=a_1=0$ leads to low-pass, while $a_2=a_0=0$ leads to band-pass. Higher order filter is implemented by cascading multiple biquads. However, at high frequencies, loading effects must be taken into consideration. In general, the input impedance of the loading stage must be much larger than the output impedance of the driving stage. The input of a transconductor ideally presents an open circuit. In practice, the preceding stage is loaded only by the impedance of the parasitic input capacitance that should be kept small enough to form a negligible load.

This approach is easy to design, can be precisely tuned and more general. They can implement any filter whose transfer function may be represented as a quotient of two polynomials (with the order of the denominator larger than or equal to that of the numerator). Filters composed of biquads may be easier to lay out, since the same floorplan may be used for different filters with only minor changes in the component value. Therefore, they are specially suited for programmable filters where the customer wants to have digital control over particular zeros or poles [4].

However, cascading biquads to achieve a high order system will suffer from its high

sensitivity to component variations. Therefore, it is not a good choice for G_m-C filter whose frequency response is determined by transconductance and capacitors, which in general cannot be matched very well in IC process.

4.3.3 Scaling

Scaling is normally necessary in the design of the filter. Scaling of a filter includes frequency scaling, impedance level scaling and dynamic range scaling. Scaling is performed to achieve an optimization between the power, area, linearity and noise.

The value of transconductance is not infinite like an opamp gain but a design parameter in a G_m-C filter. To decide how large g_m and C are needed, we first perform a transformation that multiplies all the impedances of the LC ladder by a constant factor *k*, leaves the transfer function unaltered, so that the obtained value of C is feasible [4]. Another consideration is that for layout matching purpose usually g_m and C are implemented as unit cells, which sets a lower bound on the feasible value of g_m and C.

Impedance level scaling criteria reveals that multiplying all transconductances and capacitances in a filter with a same factor *k* causes no change in frequency or quality factor of the filter. Only the impedance level is scaled. If $k>1$ then the impedance level is lowered. This results in a lower noise level that has to be paid with larger chip area and power dissipation. On the contrary, decreasing capacitance and g_m will suffer from increased noise and degraded linearity.

Frequency scaling criteria says that if in a G_m-C filter all transconductances are multiplied with a factor *k* and all capacitors are held constant, then the filter

frequency is scaled. The quality factor, determining the filter shape remains unaltered.

Finally to optimize the dynamic range of a filter, scaling of the internal signal levels is particularly important. The peaks in the internal transfer at the resonant frequency must be scaled to equal magnitude and voltage peak at the internal nodes of the filter must be eliminated to avoid increase distortion. On system level, to obtain an optimal dynamic range for a specified filter only scaling of internal signal levels and impedance level are degrees of design freedom. The scaling criterion is: the voltage levels at two nodes were halved by doubling the values of the capacitors connected at these nodes and doubling the values of any transconductor whose input is connected to these nodes, so that the rest of filter nodes is not affected [5]. On circuit level we have the freedom to minimize the transconductor distortion and noise [6].

4.3.4 A Survey of Tunable Transconductor Architectures

In a G_m-C filter, the transconductance in the G_m-C integrators are not infinite and are design parameters. The requirements for g_m cells are high DC gain, high linearity for open loop operation, low phase error. In this AAF, besides these, tenability is another challenge. If the transconductance element has no internal nodes then the transconductor circuits has no parasitic poles or zeros influencing the transfer function of the integrator. An internal node is a node in the circuit schematic that has no direct connection to either an input or an output terminal or a bias or supply terminal of the circuit. This restricts the transconductor realizations to single-stage designs. Cascading or cascoding of stages will always introduce additional internal

nodes, resulting in phase errors of the integrators [6].

Since the frequency response of a G_m-C filter is determined by G_m and C, tuning can be achieved by varying G_m or capacitors. G_m tuning allows a perfectly continuous tuning over a wide frequency range. However, wide tuning range of G_m is difficult to achieve without sacrificing the performance such as linearity and noise.

To extend the tuning range beyond the transconductor's intrinsic tuning range, G_m-switching or capacitor-switching could be implemented. G_m-switching presents some important advantages compared to capacitor-switching. Tuning capacitors is not easy to implement especially when the unit capacitance is large. In order to have a satisfactory Q for the switched capacitor array, the switch size would be very large to reduce the turn-on resistance. What's more, to preserve the filter characteristics, it is necessary to tune all the capacitors simultaneously if the filter is synthesized by passive ladder filter, which is normally the case for continuous time filter because passive ladder filter has the lowest sensitivity to process variation compared with cascading biquads. On the contrary, with G_m-switching the maximum capacitance value is always used, thus maximizing the signal-to-noise ratio. Moreover, if designed in such a way that no switch is implemented on the signal path, so any issue relative to series resistance or switch linearity is avoided [7]. As such, it would be much more efficient to tune the g_m-cell.

A tunable negative source degeneration scheme is proposed in [8], which is composed of a resistor and a positive feedback differential amplifier. By tuning the negative resistor generated by the amplifier, the g_m can be tuned over a wide range

without affecting the DC operating point of the transistors that perform the main voltage to current conversion. Tuning range of eight times is reported. However, the linearity of the positive feedback differential amplifier which is actually cross-coupled differential pair becomes the bottle neck. In [9], to achieve tuning, linear voltage to current conversion is first ensured through a fixed transconductance core, followed by a complicated tuning circuit which inevitably causes noise and power penalty. To further enhance the tuning range, G_m-switching with two transconductor banks connected in parallel is proposed in [7], one of them being switched on and off. However, extra area is occupied by the large number of g_m cells. Layout matching can be jeopardized. Effects brought by non-ideal switch cannot be ignored at high frequencies.

To conclude, continuous time filter that has a large tuning range and still maintains a high dynamic range for multi-protocol application is quite challenging.

4.3.5 Proposed Widely Tunable Transconductor

In this work, the fixed g_m core in [9] and resistor tuning to achieve g_m tuning in [8] are combined. However, instead of using active tunable negative transistors, switched-resistor arrays are utilized. Wide tuning range is achieved by the combination of discrete coarse tuning and continuous fine tuning without affecting the DC operation point, therefore preserving a good linearity over the whole tuning range. The same concept can be easily applied to the design of tunable baseband filter for multi-standard systems. The transconductor core is shown in Fig. 4.19. G_m linearity is first ensured by the use of grounded amplifier [10], which forces a linear

relationship between input voltage and current through node A+ and A-. Therefore, the transconductance stems primarily from the Z_x (impedance between node A+ and A-) with the effective G_m equal to $1/Z_x$, consequently the linearity is dominated by the implementation of Z_x. Transistor in triode region can be realized as a tunable resistor. However, its linearity is not satisfactory because of various non-idealities. In addition, when the V_g is tuned, recall that resistance for a triode region transistor is

$$R = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th} - V_{DS})} \qquad (V_{DS} < V_{GS} - V_{th}) \qquad (4\text{-}24)$$

As illustrated in Fig. 4.20, such resistance tuning bears a very limited range after V_{GS} is well above V_{th}, typically only 4 times.

Similar to the implementation of a VCO with large tuning range, a high VCO gain will inevitable degrade its noise performance. By dividing the whole range into coarse tuning and fine tuning, both wide tuning range and low phase noise can be attained. The same idea is applied to the proposed tunable transconductor cell, where 5-bit switched resistor array (SRA) is designed for coarse tuning, while a triode region transistor is added for fine tuning if continuous tuning is desired. As a result, the proposed transconductor cell can achieve a wide tuning range as large as 11 times in a compact fashion without much performance degradation and extra power penalty. In fact for many applications such as multi-band channel selection filter and the anti-aliasing filter in this work, discrete tuning is acceptable as long as bandwidth tuning resolution is fine enough. Then SRA of more number of bits can be designed to fulfill the needs, therefore eliminating the fine tuning bit. All digital bit control provides an easy interface with baseband automatic gain control (AGC) circuitry

where no A/D or D/A converters are needed. The linearity of the proposed transconductor is determined by the linearity of resistors and switches which are much better compared with active devices.

As shown in Fig. 4.19, by adding one more branch i2+ and i2-, additional output can be obtained. Dual outputs can reduce the number of g_m cells in the filter by half, while the g_m ratio can be easily scaled by altering the ratio of current mirror transistors.

The output loading utilizes diode connected PMOS transistors M1 and M2 which act as active load and define the common-mode output voltage, therefore eliminating the need of CMFB circuitry. Cross-coupled M3 and M4 form a negative resistance to enhance the output impedance, thus high DC gain. Overcompensation of R_{out} will result in a negative transconductor output resistance. In a filter this will not lead to instability problems since the transconductors will be loaded with relatively low positive impedance [6].

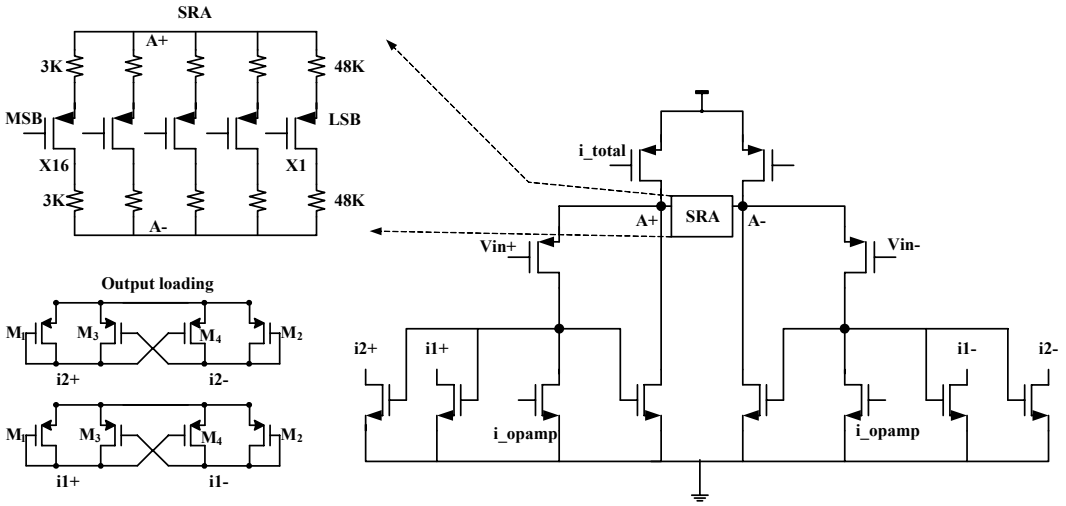


Fig. 4.19 Schematic of the proposed wide tuning g_m-cell

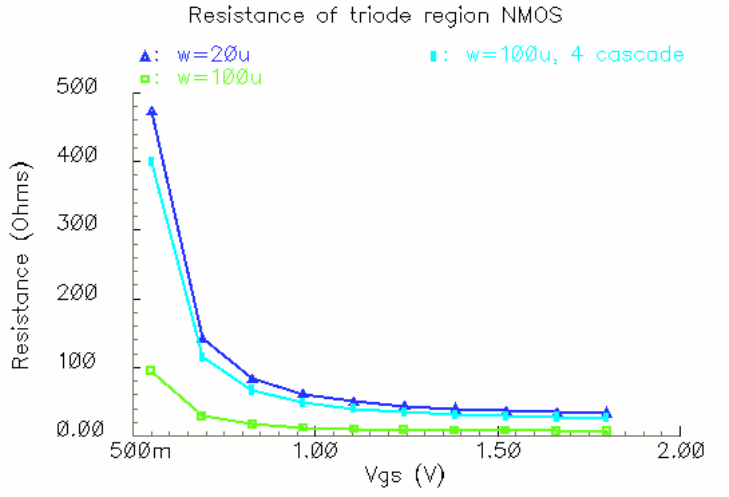
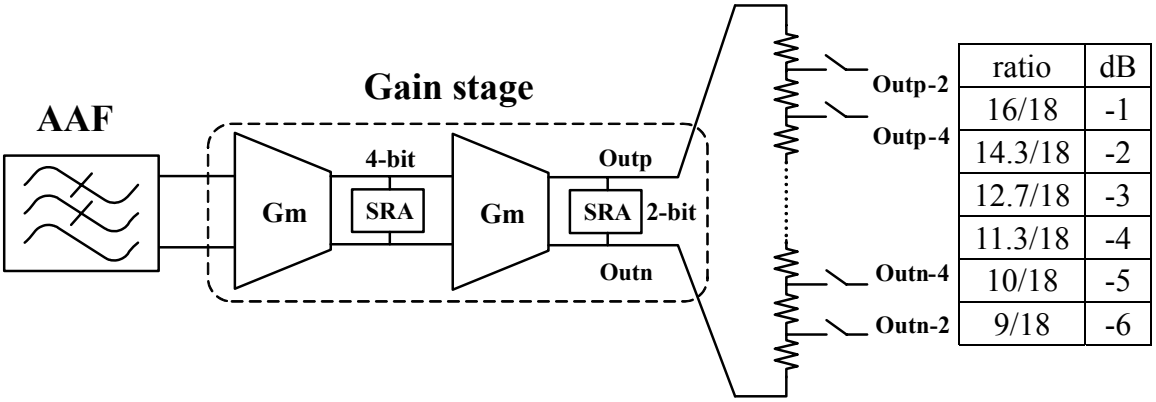


Fig. 4.20 Simulated resistance of triode region NMOS vs. V_{GS}

4.3.6 Filter Implementation

A 5th-order elliptic ladder filter prototype is chosen. The order is over-designed in order to meet the worst case anti-aliasing requirement with enough margins as well as provide partial channel selection. Gyrator method is utilized to convert the passive filter to the G_m-C filter. To implement tunable gain, a gain stage is added after the filter whose gain are given by Gain=$G_m \times R_o$, where the same g_m cell in the filter is utilized for better matching. As such, the gain can be tuned by 6dB/step by varying the R_o which is a 4-bit binary weighted SRA. Linear-in-dB gain is implemented by adding a series of resistor in parallel with the R_o and interpolating the resistor network. Since the maximum required gain of RX baseband is around 70dB, another similar variable gain stage is cascaded which includes a 2-bit binary weighted SRA. Corresponding gain setting can be selected by enabling different gain control switches. The accuracy of the 1 dB gain is determined by the ratio of resistor, which can be as good as 0.1% in IC process. Fig. 4.21 shows the gain stage and resistor ratio to get linear-in-dB gain tuning.



ratio	dB
16/18	-1
14.3/18	-2
12.7/18	-3
11.3/18	-4
10/18	-5
9/18	-6

Fig. 4.21 Gain stage with linear-in-dB resistor network and resistor ratio

As the input g_m-cell of the filter dominates the noise performance, but does not affect the filter frequency domain transfer characteristics, a separate g_m-cell with simple source degeneration architecture shown in Fig. 4.22 is adopted to minimize the noise while providing moderate linearity.

To maximize the linearity of the filter, dynamic range scaling is performed to scale the peaks in the internal transfer at around the resonant frequency to equal magnitude. Fig. 4.23 illustrates the final filter after dynamic range scaling. Three out of five g_m-cells are doubled which are denoted as $2g_m$.

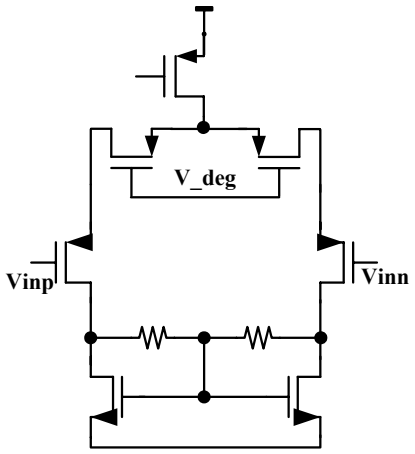


Fig. 4.22 Schematic of the input g_m-cell

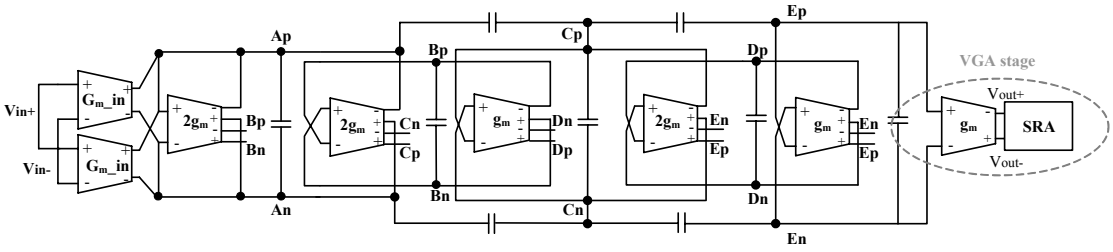


Fig. 4.23 Schematic of the whole filter

The floorplan of the G_m-C filter is illustrated in Fig. 4.24. To achieve good matching, the g_m-cells and capacitor banks are grouped into array and placed together. As can be seen in Fig. 4.23, there are only *A, B, C, D, E* five nodes in the filter. Vertical metal lines are inserted between corresponding g_m-cells while five horizontal lines run across the boundary of g_m-cells and capacitor array to ease the connection with capacitors. Since the relative matching of capacitor is not as important as the accuracy of absolute capacitance, capacitors are not interdigitated. Unit capacitance of 120fF is utilized to form large capacitance. Dummy capacitors and g_m-cells are placed at the boundary.

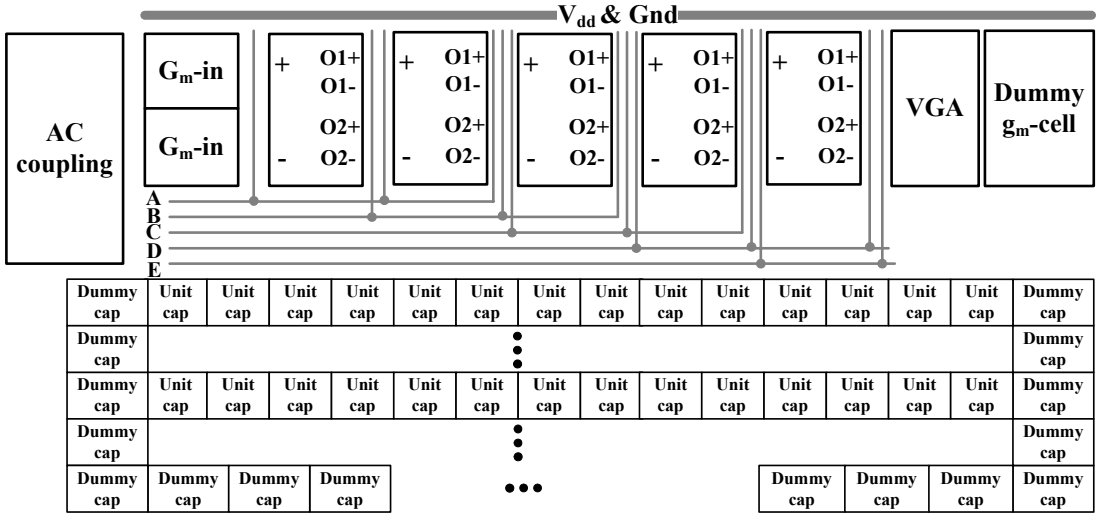


Fig. 4.24 Floorplan of the G_m-C filter

4.3.7 Experimental Results

The 5th-order elliptic low-pass filter using the proposed g_m-cell exhibits a cutoff frequency tuning range of 11 times from 145 kHz to 1.612 MHz as shown in Fig. 4.25. Fig. 4.26 is the measured gain tuning characteristic, both 6dB/step and linear-in-dB. Maximum gain is 55dB and minimum gain is 3dB. The measured noise figure is 18dB at maximum gain and maximum bandwidth, while the worst case out of band IIP3 at minimum gain and over the whole bandwidth is -3dBV. The IQ filter dissipates 9mW from a 1.8V supply.

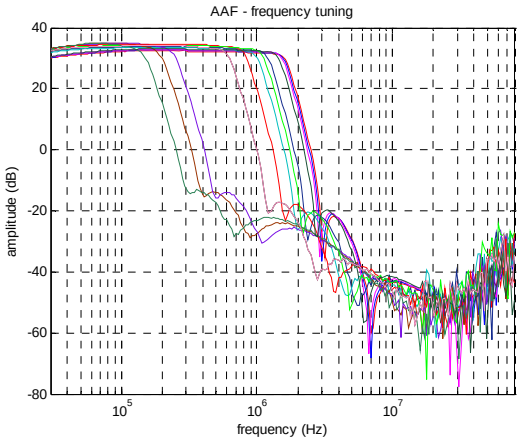


Fig. 4.25 Measured frequency tuning of the proposed anti-aliasing filter

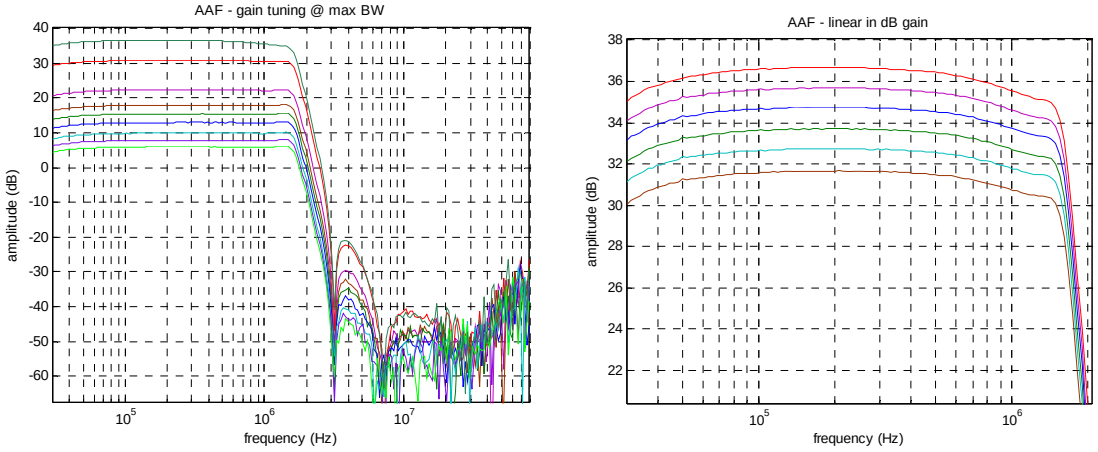


Fig. 4.26 Measured gain tuning at max bandwidth of the proposed anti-aliasing filter

4.4 Receiver Switched-Capacitor Channel Selection Filter

4.4.1 Specification and Challenges

Since the RFID system features a relative low bandwidth, in the order of 1MHz, but wide dynamic range, in the order of 70dB. Switched capacitor (SC) circuit is a suitable choice for their high precision and low distortion. The performance of SC circuits depends mainly on capacitor matching that can be controlled very well (about 0.1% with good layout technique), consequently the circuit performance is insensitive to process variation. On the other hand, the distortion in SC circuits is mainly determined by the linearity of its capacitor when the gain of the opamp is high enough. As a result, SC circuits can realize a high dynamic range compared with the continuous-time designs. Besides, bandwidth tuning can be easily achieved by changing the clock frequencies which makes it attractive for the proposed multi-protocol reader baseband.

As discussed in section 3.3.4, the CSF is able to relax the dynamic range requirement of ADC. In the mixed-mode baseband channel selection, both CSF and ADC will be implemented as switched-capacitor circuits. ADC has a dynamic range of about 51dB (9 bits) if preceding filters provides 35dB attenuation. An over-sampling ratio of 16 is enough for a 4^{th}-order ΣΔ modulator to achieve the desired dynamic range, which leads to a maximum clock frequency of ADC to be 40.96MHz.

To determine the clock frequency of the CSF, noise level in the system has to be guaranteed. When a broadband noise is sampled, the high frequency components are aliased into the frequency range of 0 to f_s, as a result, the full noise power appears in band with approximately white spectrum density [11]. The broadband resistor noise is filtered by the single-pole, lowpass filter formed by R_s (turn-on resistance of

switch) and C_s (sampling capacitor), so the total noise power at output is kT/C_s. Therefore, the noise power spectrum density is a constant: kT/C_sf_s. To keep the same noise power density, to the first order (i.e. neglect the parasitic effects), a constant C_sf_s product should be maintained. A small f_s leads to a large C_s, which results in a large capacitive load of the opamp, but longer settling time is allowed. A large f_s requires stringent settling performance, but the C_s can reduced to relax the loading. In conclusion, for a given noise requirement power of the channel selection filter is independent of f_s to the first order. The detailed analysis and calculation is the subject of Chapter 6 and can be found in section 6.1 and 6.2.

As a result, the clock frequency is chosen to be the same as that of ADC. Bandwidth is tunable from 80 kHz to 1.28MHz, which can be simply achieved by varying the f_s. The target attenuation is 25dB at 2 times the 3-dB bandwidth (another 15dB provided by trap and AAF). Maximum gain is 14dB, with tunable range of 12dB.

The challenge of the filter is to achieve desired attenuation with power consumption as low as possible.

4.4.2 Switched-Capacitor Filter Fundamentals

a) Basic Operation Principles

A switched-capacitor circuit operates as a discrete-time signal processor and finds varieties of applications in A/D and D/A converters. When applied in filtering, switched-capacitor circuits have become extremely popular due to their accurate frequency response as well as good linearity and dynamic range. Once the coefficients of a switched-capacitor discrete-time filter are accurately determined, its

overall frequency response remains a function of the sampling frequency. The basic building blocks in a switched-capacitor filter are opamps, capacitors switches and nonoverlapping clocks [11].

The fundamental working principle of switched-capacitor circuits can be well understood using a simple integrator. We assume ideal opamps with infinite DC gain, large enough unity-gain frequency and slew rate for simplicity. Fig. 4.27 shows a switched-capacitor parasitic insensitive integrator, where 1 and 2 refer to the nonoverlapping clock phase 1 and phase 2.

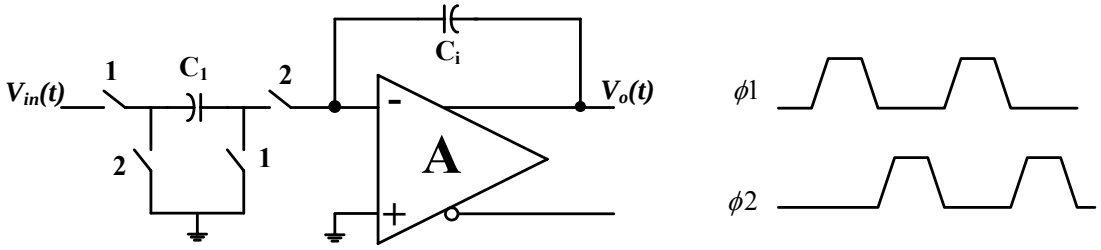
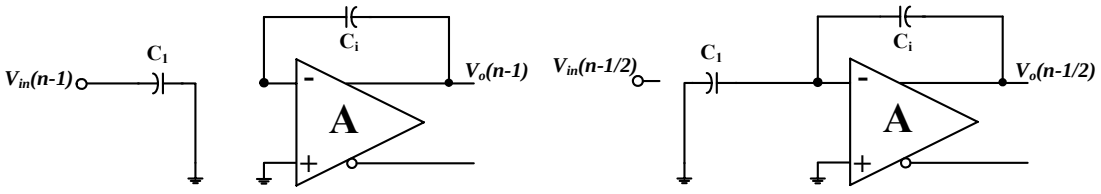


Fig. 4.27 Parasitic insensitive discrete-time integrator

Note that a virtual ground appears at the opamp's negative input. As shown in Fig. 4.28 (a), in phase 1, an initial integrator output voltage of $V_o(n-1)$ implies that the charge on C_i is $C_iV_o(n-1)$. At the same time the input signal $V_{in}(n-1)$ is sampled, and the charge of $C_1V_{in}(n-1)$ is stored on C_1. When $\phi 2$ goes high, C_1 is forced to discharge through the virtual ground node, and the discharging current passes through C_i hence the charge on C_1 is added to the charge already present on C_i.



(a) (b)

Fig. 4.28 The discrete-time integrator for two phases: (a) $\phi 1$, (b) $\phi 2$

To obtain the transfer function, time domain analysis is performed using Kirchhoff Charge Law [12]. Table 4.2 summaries the detailed charge transfer at all capacitors.

Table 4.2 Timing diagram showing charge transfer at all capacitors

Cap	ϕ1=1, [(n−1)T, (n-1/2)T]	ϕ2=1, [(n-1/2)T, nT]	ϕ1=1, [nT, (n+1/2)T]
C_1	$V1(n-1)=V_{in}(n-1)$	$V1(n-1/2)=0$	$V1(n)=V_{in}(n)$
C_i	$Vi(n-1)=-V_o(n-1)$	$Vi(n-1/2)=-V_o(n-1/2)$	$Vi(n)=-V_o(n)$

During clock phase transition, the total charge is conserved, i.e., the sum of the change of the charge in capacitors is 0. We have

$$C_1[0-V_{in}(n-1)]=C_i[-V_o(n-1/2)+V_o(n-1)] \tag{4-25}$$

Note that during ϕ2, the following holds

$$V_o(n-1/2)=V_o(n) \tag{4-26}$$

Apply the Z-transform, the transfer function can be written as

$$H(z)=\frac{V_o}{V_{in}}=\frac{C_1}{C_i}\frac{z^{-1}}{1-z^{-1}} \tag{4-27}$$

Similar analysis can be performed for an opamp with finite gain. The only difference is that the opamp input node is no longer virtual ground but with a finite voltage of V_o/A, where A is the opamp gain. Table 4.3 shows the detailed charge transfer at all capacitors for an opamp with finite gain A.

Table 4.3 Timing diagram showing charge transfer at all capacitors with finite gain opamp

Cap	ϕ1=1, [(n−1)T, (n-1/2)T]	ϕ2=1, [(n-1/2)T, nT]	ϕ1=1, [nT, (n+1/2)T]
C_1	$V1(n-1)=V_{in}(n-1)$	$V1(n-1/2)=V_o(n-1/2)/A$	$V1(n)=V_{in}(n)$
C_i	$Vi(n-1)= -V_o(n-1)/A$ $-V_o(n-1)$	$Vi(n-1/2)= -V_o(n-1/2)/A$ $-V_o(n-1/2)$	$Vi(n)= -V_o(n)/A$ $-V_o(n)$

The total charge is still preserved, so we have

$$C_1[\frac{V_o(n-1/2)}{A}-V_{in}(n-1)]=C_i[-\frac{V_o(n-1/2)}{A}-V_o(n-1/2)+\frac{V_o(n-1)}{A}+V_o(n-1)]$$

(4-28)

Substituting (4-26) into (4-28) and simplifying results in

$$H(z) = \frac{V_o}{V_{in}} = \frac{C_1}{C_i} \frac{z^{-1}}{(\frac{1}{A}+1)(1-z^{-1}) + \frac{C_1}{C_i A}} \tag{4-29}$$

It is observed that the finite gain of the opamp reduces the integrator gain and causes relative phase error [12].

Using signal flow graph, 1st-order filter can be easily synthesized [11]. Higher order filter is usually obtained by cascading biquads. Because of the high accuracy in implementing the transfer function using switched-capacitor technique, cascading biquad approach is more prevalent as compared with continuous time filter.

b) Non-ideal Impacts on Switched-Capacitor Filter

In previous example, the non-ideal effect on the switched-capacitor filter has been discussed such as finite gain of the opamp. Not only that, when the effects of the amplifier dynamics, such as opamp's finite bandwidth and slew rate are considered, the situation is even worse. The unity-gain frequency and phase margin of an opamp indicates the small signal settling behavior of an opamp. A general rule of thumb is that the clock frequency should be at least five times lower in frequency than the unity-gain frequency of the opamp assuming little slew-rate behavior occurs and phase margin greater than 70 degrees [11]. The finite slew rate can limit the settling as switched-capacitor circuits reply on charge being quickly transferred from one capacitor to another.

Ideal switch has very high off resistance so that charge leakage is small, but a low on

resistance so that circuit can settle fast and introduces no offset voltage when turned on. Although MOSFET transistor, especially the transmission gate performs quite satisfactorily as a switch, it still imposes some non-ideal effects. For example, to reduce the on resistance, the W/L ratio needs to be large, which cause large transistor size thus large parasitic capacitance. Besides, the nonlinear parasitic capacitance can couple the clock transitions to the sampling capacitor. Depicted in Fig. 4.29, the effect is called clock feedthrough, which introduces an error in the sampled output voltage.

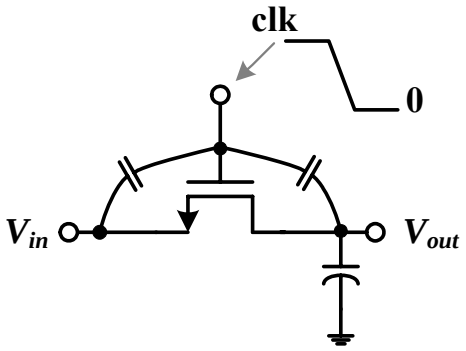


Fig. 4.29 Clock feedthrough due to switch parasitic capacitance

The charge accumulated in the channel of a switch when it is on injects to the sampling capacitors when it is off and causes gain error, dc offsets and nonlinearity. This phenomenon is called channel charge injection [13]. It can be reduced by careful switch timing, a scheme called bottom plate sampling. By disconnecting some critical capacitors slightly before turning off the actual switch and avoiding any current path for charge injection, the effect of the non-ideal switches is minimized, hence quite accurate transfer function is guaranteed.

4.4.3 Filter Circuit Design and Layout

a) Finite Gain and Offset Compensation

High gain and high bandwidth opamp is in general difficult to realize and power hungry. Simple gain and offset cancellation proposed in [14] can be applied to relax the gain of the opamp therefore reducing the power dissipation.

The principle can be illustrated in Fig. 4.30. If we can store the residual error caused by the finite opamp gain and cancel it during the integration phase, a perfect virtual ground is ensured. Thus the effect of the finite opam gain is compensated as well as the input offset voltage of the opamp.

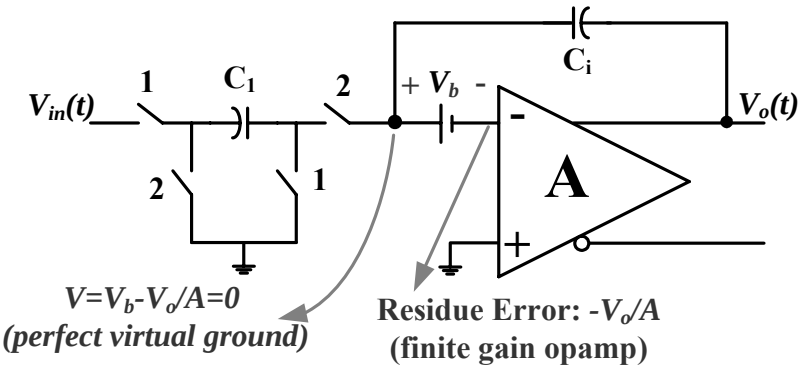


Fig. 4.30 Working principle of the finite gain and offset compensation technique

As discussed in section 4.4.1, in this project the sampling frequency of the CSF is chosen to be the same as that of the oversampling ΣΔ ADC, therefore the filter has quite low cutoff frequencies compared to the sampling frequency. Depicted in Fig. 4.31, it is possible to add a capacitor to store the output in the sampling phase $V_o(n-1)/A$ and cancel the error in integration phase $V_o(n-1/2)/A$ if we assume the output voltage changes little during these two phases, i.e.: $V_o(n-1) \approx V_o(n-1/2)$. This technique is applied in the proposed CSF to relax the opamp gain from about 60dB to around 40dB.

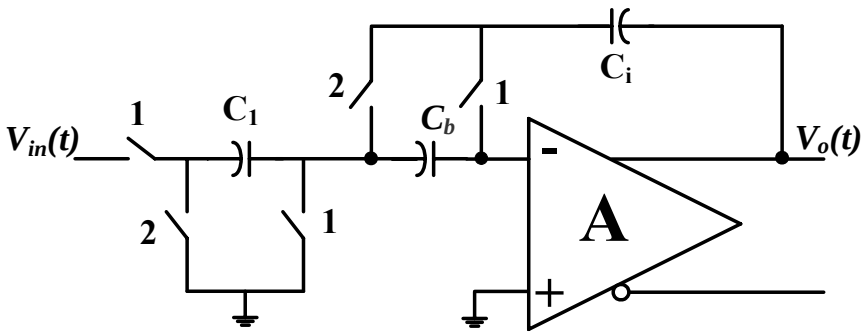


Fig. 4.31 Schematic of the integrator with finite gain and offset compensation

b) 1st-Order Low-Pass Filter

A 3rd-order CSF is constructed by cascading one 1st-order lowpass filter and one biquad. The sampling capacitor of the first stage needs to be considered carefully because its kT/C noise dominates the noise performance. Later stages can adopt minimum sampling capacitors to relax the opamp loading due to the gain of the first stage. A simple 1st-order lowpass filter is chosen as the initial stage of the CSF. The focus is tunable gain, acceptable noise rather than sharp roll-off. For the target input referred noise power of 5.3e-9V^2 and f_s of 40.96MHz, the sampling capacitor of 300fF is found enough, detailed derivation can be found in section 6.2.

The desired filter transfer function is obtained by matlab,

$$H_1(z) = \frac{4}{5}\frac{z+1}{z+(\frac{2}{5}-1)} \tag{4-30}$$

Then a proper architecture is synthesized that can generates the lowpass function as shown in Fig. 4.32. Finite gain and offset compensation technique is applied and the number of switches is minimized by sharing and eliminating unnecessary switches. Further, bottom plate sampling technique is employed to reduce the effect of charge injection and clock feedthrough by turning off certain switches slightly earlier which are controlled by clock phase 1C and 2C as illustrated in Fig. 4.32.

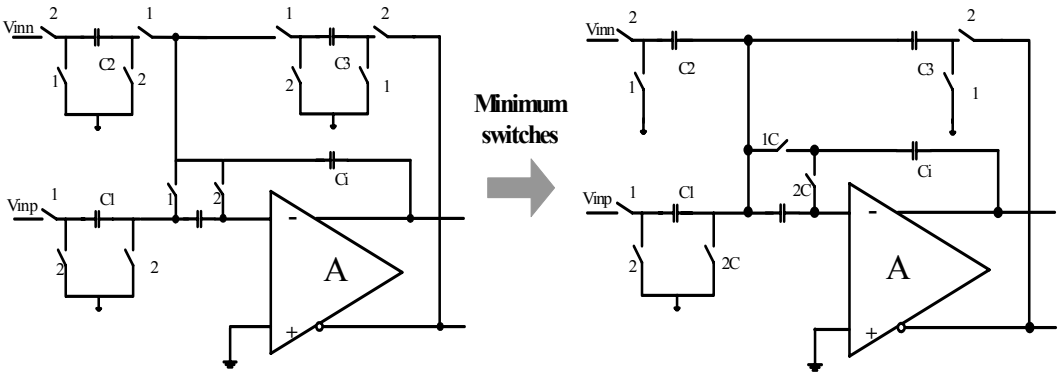


Fig. 4.32 Schematic of the 1st-order low-pass filter

The transfer function can be derived based on the time domain analysis introduced in 4.4.2 a). Table 4.4 shows the charge transfer at all capacitors.

Table 4.4 Detailed charge transfer at all capacitors of 1st-order lowpass filter

	ϕ1→ ϕ2		ϕ2→ ϕ1
Cap	ϕ1＝1，[(n-1)T,(n-1/2)T]	ϕ2=1,[(n-1/2)T,(n)T]	ϕ1=1,[(n)T,(n+1/2)T]
C_1	V1(n-1)=Vinp(n-1)	V1(n-1/2)=0	V1(n)=Vinp(n)
C_2	V2(n-1)=0	V2(n-1/2)=Vinn(n-1/2)	V2(n)=0
C_3	V3(n-1)=0	V3(n-1/2)=-Von(n-1/2)	V3(n)=0
C_i	Vi(n-1)=-Vop(n-1)	Vi(n-1)=-Vop(n-1/2)	Vi(n)=-Vop(n)

According to KQL

$$\Delta C_1 + \Delta C_2 = \Delta C_3 + \Delta C_i \tag{4-31}$$

Therefore we have

$$C_1(V_{inp}(n)) + C_2(-V_{inn}(n-1/2)) = C_3(V_{on}(n-1/2)) + C_i(-V_{op}(n) + V_{op}(n-1/2)) \tag{4-32}$$

Note that at the start and the end of ϕ1, the following holds

$$V_o(n-1) = V_o(n-1/2) \tag{4-33}$$

Substituting (4-33) into (4-32) and simplifying results in

$$\frac{V_{op}}{V_{inn}} = \frac{C_1}{C_i} \frac{z + \frac{C_2}{C_1}}{z + (\frac{C_3}{C_i} - 1)} \tag{4-34}$$

Variable gain is implemented by changing the C_1 using two binary weighted switches,

therefore 6dB/step and 12dB total gain tuning range is realized. As can be seen from the schematic in Fig. 4.32, the feedback factor in integration phase is given as

$$\beta = \frac{C_i}{C_1 + C_2 + C_3 + C_i} \tag{4-35}$$

Too large a gain which means large C_1 and C_2 reduces the feedback factor hence makes the settling more stringent.

c) Biquadratic filter

The biquad is modified from [15] so that finite gain and offset compensation technique is applied. The schematic is shown in Fig. 4.33. This biquad architecture breaks all direct charge transfer paths between the two opamps, thus synthesize transmission zeros without global feedback which would significantly improve the operation speed. Transmission zeros can result in fast attenuation. It is well-known that elliptic filter has a much larger attenuation than the all pole filters such as buttorworth and chebyshev with the same order. Further, bottom plate sampling technique is employed to reduce the effect of charge injection and clock feedthrough by turning off certain switches slightly earlier which are controlled by clock phase 1C and 2C as illustrated in Fig. 4.33.

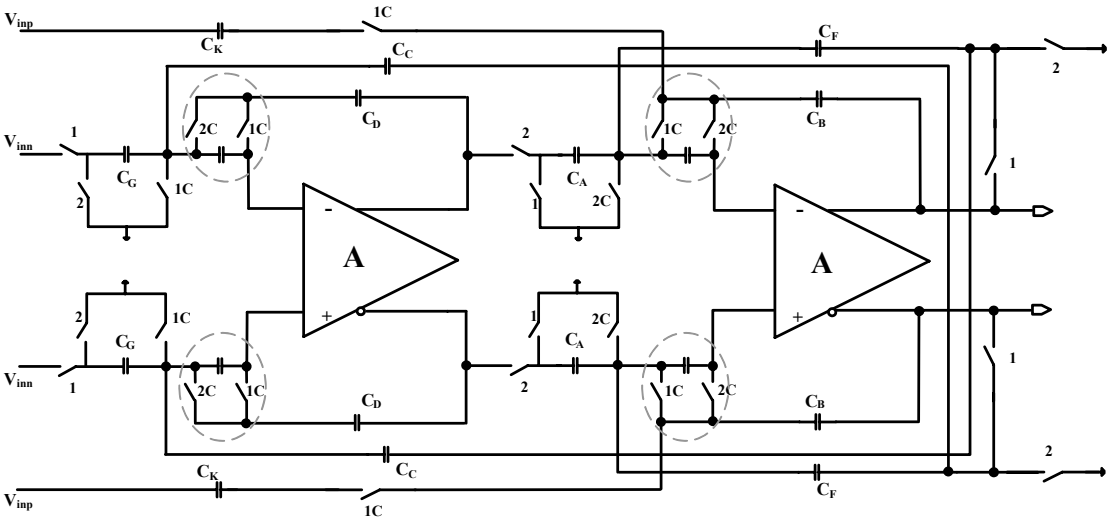


Fig. 4.33 Schematic of the biquad

The transfer function can be derived based on the time domain analysis introduced in 4.4.2 a). Table 4.5 shows the charge transfer at all capacitors.

Table 4.5 Detailed charge transfer at all capacitors of biquad

	$\phi1 \rightarrow \phi2$		$\phi2 \rightarrow \phi1$
Cap	$\phi1=1$, [(n-1)T,(n-1/2)T]	$\phi2$=1,[(n-1/2)T,(n)T]	$\phi1$=1,[(n)T,(n+1/2)T]
C_A	Va(n-1)=0	Va(n-1/2)=Vo1(n-1/2)	Va(n)=0
C_B	Vb(n-1)=-Vop(n-1)	Vb(n-1/2)=-Vop(n-1/2)	Vb(n)=-Vop(n)
C_C	Vc(n-1)=-Von(n-1)	Vc(n-1/2)=0	Vc(n)=-Von(n)
C_D	Vd(n-1)=-Vo1(n-1)	Vd(n-1/2)=-Vo1(n-1/2)	Vd(n)=-Vo1(n)
C_F	Vf(n-1)=-Vop(n-1)	Vf(n-1/2)=0	Vf(n)=-Vop(n)
C_G	Vg(n-1)=Vinn(n-1)	Vg(n-1/2)=0	Vg(n)=Vinn(n)
C_K	Vk(n-1)=Vinp(n-1)	Vk(n-1/2)=Vinp(n-1)	Vk(n)=Vinp(n)

According to KQL

$$\Delta C_G = \Delta C_D + \Delta C_C \tag{4-36}$$

$$\Delta C_A + \Delta C_K = \Delta C_B + \Delta C_F \tag{4-37}$$

Therefore we have

$$C_G(-V_{inn}(n-1)) = C_D(-V_{o1}(n-1/2) + V_{o1}(n-1)) + C_C(V_{on}(n-1)) \tag{4-38}$$

$$C_A(-V_{o1}(n-1/2)) + C_K(V_{inp}(n) - V_{inp}(n-1)) = C_B(-V_{op}(n) + V_{op}(n-1/2)) + C_F(-V_{op}(n)) \tag{4-39}$$

Note that at the start and the end of ϕ1 and ϕ2, the following hold

$$V_{op}(n-1) = V_{on}(n-1/2) \tag{4-40}$$

$$V_{o1}(n) = V_{o1}(n-1/2) \tag{4-41}$$

Substituting (4-40), (4-41) into (4-38), (4-39) and simplifying results in

$$C_D V_{o1}(1-z^{-1}) = C_G V_{inn} z^{-1} - C_C V_{op} z^{-1} \tag{4-42}$$

$$C_B V_{op}(1-z^{-1}) = C_A V_{o1} - C_F V_{op} + C_K V_{inn}(1-z^{-1}) \tag{4-43}$$

Finally we obtain the transfer function of the biquad

$$\frac{V_{op}}{V_{inn}} = \frac{C_K}{(C_B + C_F)} \frac{Z^2 + (\frac{C_A C_G}{C_D C_K} - 2)Z + 1}{Z^2 + (\frac{C_A C_C}{C_D(C_B + C_F)} - \frac{C_F}{(C_B + C_F)} - 2)Z + \frac{C_B}{(C_B + C_F)}} \tag{4-44}$$

To achieve target attenuation, the desired 2nd-order elliptic transfer function is first calculated by matlab,

$$H_2(z) = \frac{24z^2 - 43.52z + 24}{48z^2 - 82.08z + 37.44} \tag{4-45}$$

The next step is to calculate the final desired capacitance value based on (4-44) and (4-45). There are several constraints: 1) minimum capacitor or unit capacitor is in the order of 50fF for accuracy consideration; 2) As can be seen from (4-44), the poles and zeros depend on three capacitor ratios: C_A/C_D, C_G/C_K and $C_C/(C_B+C_F)$. As long as good matching is ensured in each group, accurate transfer function can be obtained. Therefore, different unit capacitors can be used; 3) dynamic range optimization has to be performed to ensure the two opamp outputs have the same peak value to avoid distortion. The final designed value of capacitors is summarized in table 4.6.

Table 4.6 Final implemented capacitance of the biquad

Cap	Calculated Value (fF)	Design value (fF)	Cap	Calculated Value (fF)	Design value (fF)
C_A	89.6	60+60/2	C_B	249.6	60×3+(60+80)/2
C_D	240	60×4	C_C	60	60
			C_F	70.4	(60+80)/2
C_G	80	80			
C_K	160	80×2			

Fig 4.34 shows the matlab calculated transfer function of 1st-order low-pass filter, biquad and the CSF when gain is maximal.

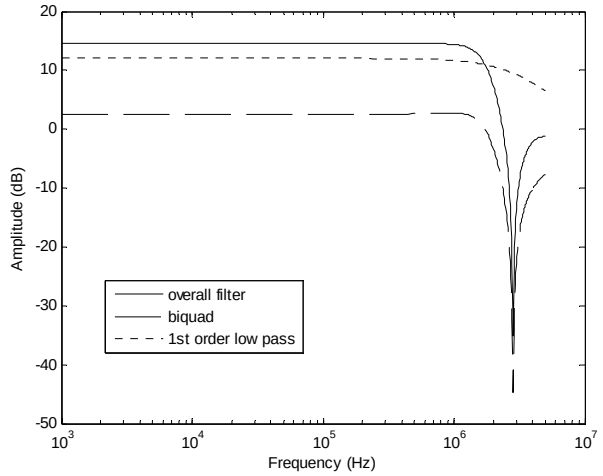


Fig. 4.34 Calculated frequency response of the CSF

SWITCAP behavior simulation is then performed. Fig. 4.35 illustrated the simulated CSF transfer function without gain-and-offset compensation (GOC) technique, ideal opamp and with gain-and-offset compensation (GOC) technique, opamp gain of 40dB. Negligible errors are observed, which proves the effectiveness of this technique. The dynamic range optimization in the biquad is also shown in Fig. 4.35. The peaks of the two outputs of the biquad are scaled to similar value for largest dynamic range.

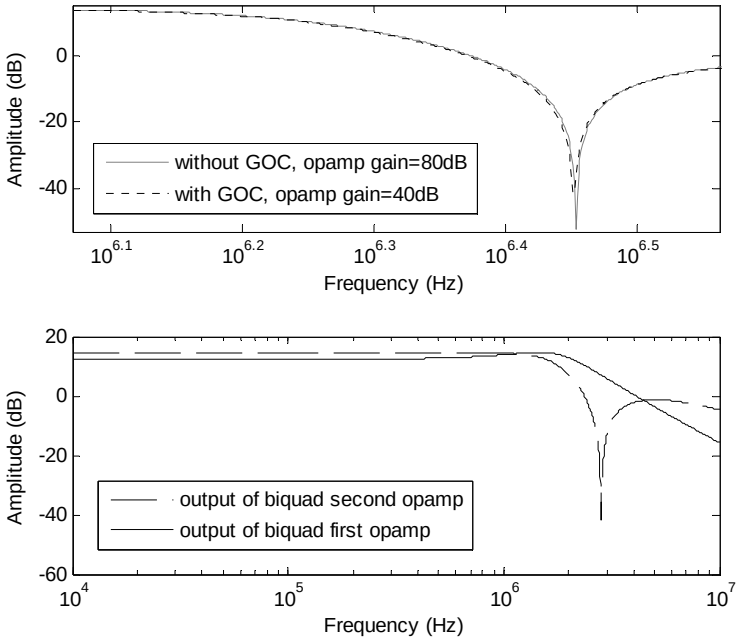


Fig. 4.35 SWITCAP behavior simulation result

d) Operational Transconductance Amplifier

The impact of the non-idealities of the opamp on the overall filter performance is discussed in section 4.4.2. Therefore, the specification of the opamp should be decided such that the non-idealities pose negligible effects on the filter performance. The key specifications are DC gain, phase margin, unity-gain frequency, slew rate, etc. After the specification of the opamp is derived, a proper architecture should be chosen to fulfill the requirement.

The target DC gain of the opamp is 40dB according to the SWITCAP simulation result. The phase margin is designed to be 60° to avoid stability issues.

In switched capacitor circuits, the opamp is connected in the feedback configurations. A generic structure of opamp in feedback configuration is illustrated in Fig. 4.36.

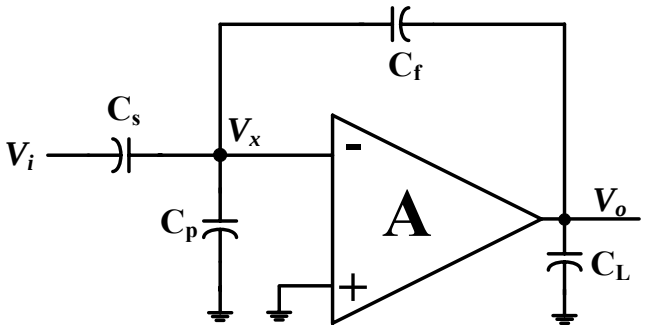


Fig. 4.36 Generic opamp in a feedback configuration

According to KCL, we have

$$(v_i - v_x)sC_s + (v_o - v_x)sC_f - v_x sC_p = 0 \tag{4-46}$$

$$g_m v_x + v_o sC_L + (v_o - v_x)sC_f = 0 \tag{4-47}$$

Thus we obtain the transfer function

$$\frac{v_o}{v_i} = \frac{C_s(1-\frac{sC_f}{g_m})}{1+s\frac{C_L+(1-F)C_f}{g_m F}} = C_s\frac{1-p}{1-z} \tag{4-48}$$

Where F is the feedback factor defined as

$$F = \frac{C_f}{C_s + C_p + C_f} \tag{4-49}$$

While the pole and zero is

$$p = \frac{g_m}{C_f} \tag{4-50}$$

$$z = -\frac{g_m F}{C_L + (1-F)C_f} \tag{4-51}$$

The effective loading capacitor of the circuit is given as

$$C_{Leff} = C_L + \frac{C_f \times (C_s + C_p)}{C_f + C_s + C_p} = C_L + (1-F)C_f \tag{4-52}$$

If a step impulse is applied to the circuit in Fig. 4.36, the settling behavior can be studied by multiplying V_{step}/S to (4-48) in S-domain and performing the Inverse

Laplace Transform to get the time domain response.

$$V_{o,step}(t) = -V_{step}C_s[1-(1-\frac{p}{z})e^{-t/\tau}] \tag{4-53}$$

Where τ is the time constant

$$\tau = \frac{C_{Leff}}{Fg_m} \tag{4-54}$$

To achieve 0.1% settling error, the required setting time is about 7τ. If we design the settling time of the opamp to be less than 40% of the sampling time (minimum sampling time is 12.2ns at 40.96MHz), we have

$$\tau = \frac{C_{Leff}}{Fg_m} = \frac{1}{F \cdot UGF \cdot 2\pi} \le \frac{12.2ns \times 0.4}{7} \tag{4-55}$$

Thus the minimum unity gain frequency (UGF) to meet the settling requirement is

$$UGF \ge \frac{10^9}{4.38F} \tag{4-56}$$

The response of an operational amplifier that employs a differential pair as its input stage typically includes a slew limited region followed by a linear settle region [16]. The linear settling region is dominated by the time constant τ as discussed, while in the slew limited region, settling is dominated by the opamp's slew rate. The sum of the time time duration shouldn't exceed the sampling period, i.e. *1/2*f_s. If the slew limited region is designed to be less than 20% of the sampling period, for an maximum differential output swing of 1.2V, the slew rate must be larger than 1.2/(0.2×12.2ns)=0.49V/ns.

The largest load capacitor is found to be about 800fF by looking at the effective loading capacitor at the output of three opamps in each phase. While the worse case feedback factor is 0.56 which occurs at the third opamp. Up to now, we are able to

get all the specifications of the opamp as summarized in table 4.7.

Table 4.7 Summary of the specification of the opamp

Parameters	Specification
Supply voltage	1.8V
DC gain	40dB
Unity gain frequency	457MHz
Phase margin	60°
Differential output swing	1.2V
Slew rate	0.49V/ns
Load capacitor	800fF

For high speed, moderate gain, current mirror opamp is a good candidate and hence adopted in this design. Fig. 4.37 illustrates the schematic of the opamp.

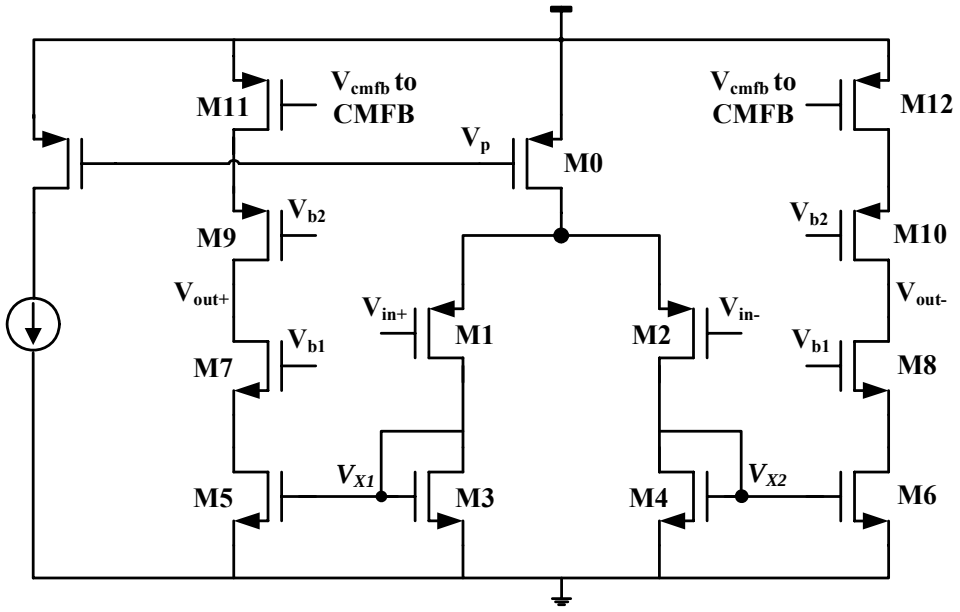


Fig. 4.37 Schematic of the opamp

Without cascode in the output branch, the DC gain can merely exceed 40dB though the channel length is increased to 0.6μm. Such big device also hurts the frequency response, since the parasitic capacitance is much larger. As a result, cascode configuration is implemented in the output to achieve 40dB gain with the minimum channel length to improve the speed at the cost of reduced output swing.

In this opamp architecture, the second dominant pole is generated at node V_{X1} and

V_{X2}. To maximize the 2nd dominant pole for larger unity gain frequency, large g_m of M3 and M4 is required. Therefore, PMOS input transistor is chosen so that the NMOS M3 and M4 have larger g_m than their PMOS counterpart. However it results in larger input capacitance of the opamp. For current mirror opamp, larger current ratio K of the output and input branch brings larger unity gain frequency and slew rate. However, increasing the K increases the total capacitance at node V_{X1} and V_{X2}, therefore reduces the frequency of the 2nd dominant pole. Finally, K is chosen to be 1.5 as an optimal value. For high speed, all the transistors use minimum channel length (0.18μm) except current mirror transistor M0 to enhance the common-mode rejection ratio.

Fig. 4.38 shows the simulated gain and phase response of the opamp. The DC gain is 51dB, while the phase margin is 57° at the unity gain frequency of 1.1GHz.

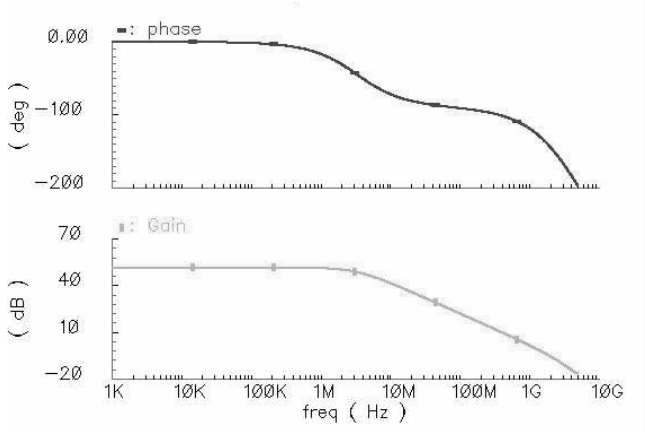


Fig. 4.38 Simulated gain and phase response of the opamp

The simulated transient response of the opamp for a differential input signal (1.8V) is shown in Fig. 4.39. The positive slew rate is 0.94V/ns, while the negative slew rate is 0.92V/ns. The opamp is slightly overdesigned since the previous calculation doesn't take the parasitic capacitor and loading of CMFB circuit into account. The opamp

consumes 3mA from a 1.8V supply.

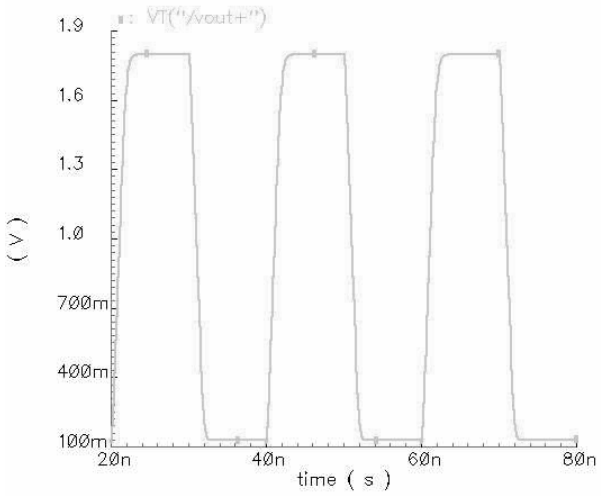


Fig. 4.39 Slew rate simulation results of the opamp

e) Switched-Capacitor Common-Mode Feedback Circuit

Opamp with fully differential topology provides much better rejection of common-mode (CM) noise and high frequency power supply variations compared to their single-ended counterparts. However, since the CM loop gain from the external feedback loop around the fully-differential opamp is small, the CM voltage is not precisely defined. Hence, a CMFB circuit is required to control the output voltage.

Switched-capacitor CMFBs are commonly used in switched-capacitor circuits. The main advantage of the switched-capacitor CMFB are that they impose no restrictions on the maximum allowable differential input signals, have no additional parasitic poles in the CM loop, and are highly linear. Nevertheless, SC-CMFBs inject nonlinear clock feedthrough noise into the opamp output nodes and increase the load capacitance that needs to be driven by the opamp [16]. Fig. 4.40 illustrates the schematic of the SC-CMFB.

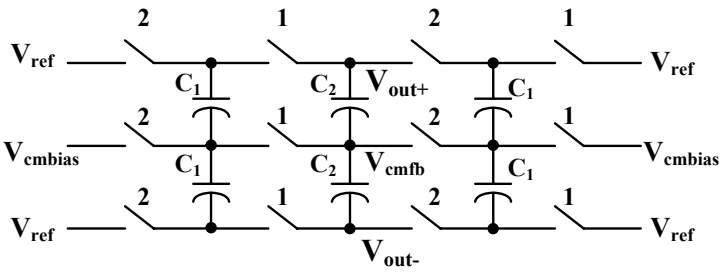


Fig. 4.40 Schematic of the SC-CMFB

Depicted in Fig. 4.40, the basic working principle of SC-CMFB is sensing the output CM and comparison with a reference voltage directly with capacitors precharged to a desired offset voltage. In particular, this architecture has the benefit that switches operate with opposite clock phase and present a symmetric loading (C_1+C_2) on the differential loop during every clock phase. Complementary switches are utilized in the SC-CMFB since the V_{ref} is 0.9V and V_{cmbias} is about 1V.

f) Clock and Phase Generator

Illustrated in Fig. 4.41, since bottom plate sampling is applied, four pairs of clock phases are required in view of the complementary clock phases required by both the NMOS and PMOS transistors.

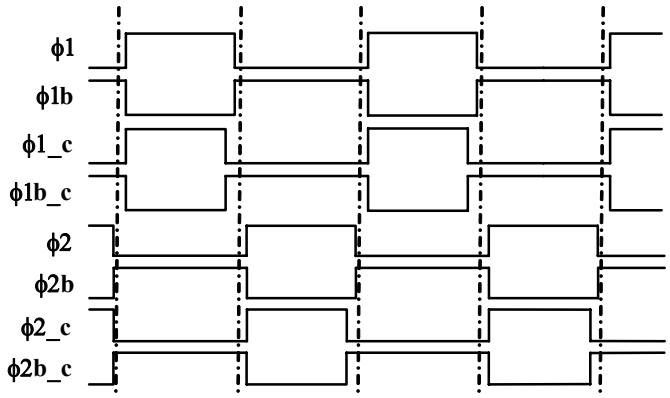


Fig. 4.41 Four pairs of clock phases required in the CSF

The clock phases are generated on-chip from a single external master clock. Fig. 4.42 shows the schematic of the clock generator. The output clock signals are connected to

buffer chains to drive the switches in the filter.

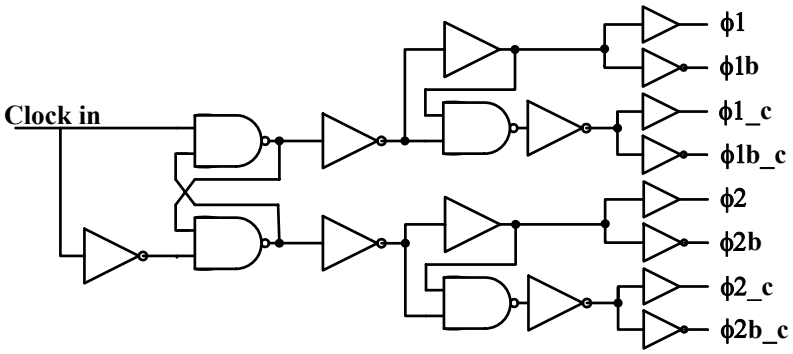


Fig. 4.42 Schematic of the clock phases generator

g) Layout Consideration

As one of the mixed-signal circuit, the layout floorplan of the switched-capacitor circuits needs to be carefully considered. In particular, the input terminal of the opamp is most sensitive to noise so that it should be kept silent. Consequently any coupling from the digital part through parasitic capacitance should be avoided [12]. As shown in Fig. 4.43, the analog part of the circuit consists of opamps, switches and capacitors. To minimize the noise due to the digital circuits, a ground-shielded guard ring is inserted in between the analog parts and clock buses. MOS caps of large value are put under the digital VDD and bias voltages as decoupling capacitor.

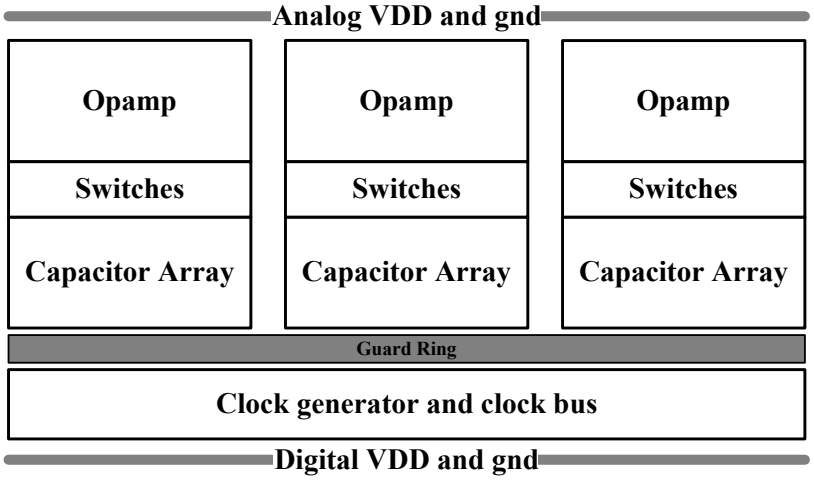


Fig. 4.43 Layout floorplan of the CSF

Since good matching of capacitor is a must for accurate filter transfer function, all the capacitors that need to be matched are placed close to each other. The best matching can be achieved if all the capacitors are designed to be an integer number of the unit capacitance. What's more, the unit capacitor is drawn in square shape to minimize the capacitance error due to over-etching [16]. To match two capacitors with non-integer ratio, the ratio of the perimeter to area of the two capacitors should be kept the same. As listed in table 4.6, in biquad, unit square capacitance is chosen as 60fF, while the 80fF unit cap is in rectangular shape with its length and width calculated according to the above criterion. In the 1st-order lowpass filter, the unit cap is 100fF in square shape.

4.4.4 Experimental Results

Sampled at 40.96MHz, the 3rd-order switched-capacitor filter achieves a maximum gain of 11dB and attenuation of 20dB at adjacent channel as illustrated in Fig. 4.44. The out of band IIP3 is 6dBV. The total power consumption of the IQ CSF can be optimized from 30mW when sampled at 40.96MHz to 1.95mW when sample frequency reduced to 2.56MHz.

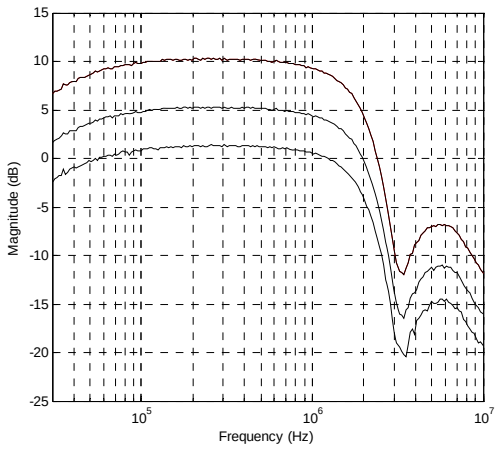


Fig. 4.44 Measure frequency response and gain tuning of the CSF

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Chapter 5

DESIGN AND MEASUREMENT OF THE OTHER BUILDING BLOCKS IN THE READER TRANSCEIVER

5.1 Introduction

In previous chapters, the reader architecture and unique features are discussed. In particular, a low power low phase noise synthesizer is proposed and a highly reconfigurable baseband is designed to facilitate multi-protocol operation in terms of power, bandwidth and interference rejection ability. In addition, the proposed reader integrates a highly linear RX front-end, IQ ΣΔ A/D converters, IQ current steering D/A converters, RF variable gain amplifier (RF-VGA) and digital baseband as shown in Fig. 5.1. In this chapter, the design and measurement of these building blocks will be briefly introduced.

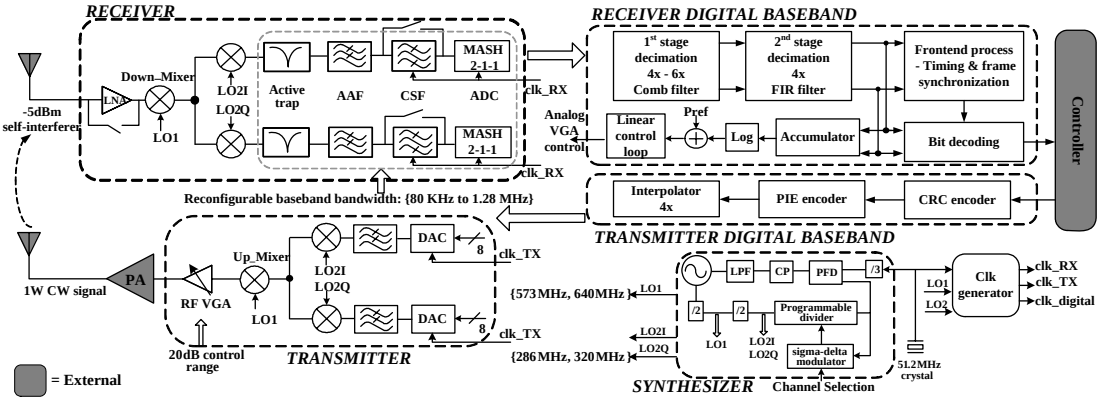


Fig. 5.1 Architecture of the proposed RFID reader

5.2 Receiver Building Blocks

5.2.1 Low Noise Amplifier

a) Circuit Design

In the RFID receiver, due to the large self-interference, the front-end linearity is stringent. Moreover, it can only afford to have limited gain to avoid saturation. As such, the main focus on the LNA design is not high gain low noise but high linearity with moderate gain and noise.

Transconductance and output conductance are two dominant nonlinear sources of MOSFETs. There are several existing solutions for LNA linearization, most of which focus on linearizing transconductance. Feedforward technique proposed in [1] has a main path and a 3^{rd}-order intermodulation (IM3) cancellation path. It cancels IM3 by summing two outputs which have the same amplitude and the opposite phase in IM3s. However, the input signal for the cancellation path has to be several times larger and in-phase with the input of main path, thus hard to generate on-chip. In addition, the cancellation path degrades the overall gain and consumes the same power as the main path. The multiple gated transistor linearization [2] utilizes the characteristic of 180^{o} IM3 phase difference between two differently gate-biased transistors, combines the two transistors' drain current and achieves IM3 cancellation. However, this linearization depends on the device physical characteristic, hence large input power level may affect the characteristic and degrade the cancellation. These existing solutions linearize the circuit by current summing of main and cancellation paths at the output. By doing so, both gain and NF of the main amplifier may be affected,

which complicates the design. Adaptively biased transconductor has been reported for long [3]. The constant bias current of the differential pair is replaced by a signal dependent bias current that is proportional to the square of the input signal, which can completely eliminate distortion for a square-law device. Unfortunately, the frequency response of this linearization is poor because the output from the squaring circuit has to propagate around the feedback loop before it is applied to the differential pair. As a result, the linearity improvement is only evident at low frequencies.

In this work, a linearization technique with low-frequency 2nd-order IM product (IM2) injected to the current source of the differential pair is proposed to achieve IM3 suppression without affecting gain, NF while only consuming little power. The schematic of the LNA with a proposed linearization technique is shown in Fig. 5.2.

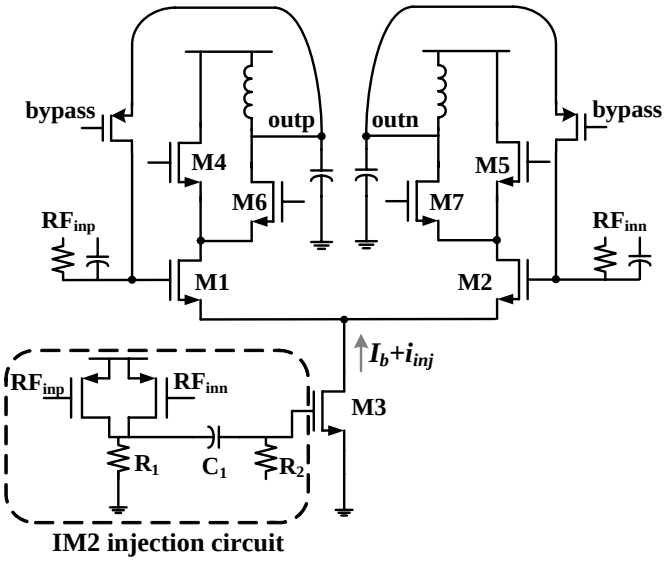


Fig. 5.2 Schematic of the proposed LNA

The non-linearity of a MOS transistor can be investigated by modeling its IV characteristic as:

$$i_d = g_1(v_g - v_s) + g_2(v_g - v_s)^2 + g_3(v_g - v_s)^3 + \ldots \quad (5\text{-}1)$$

where g_i represents the i[th]-order transconductance coefficient of the input device, and v_g and v_s are the gate and source voltages. It can be shown that for two input tones located at ω_1 and ω_2 with equal magnitude of A, if a low-frequency 2[nd]-order intermodulation (IM2) current i_{inj} is injected to the bias transistor M3, the third-order intermodulation term IM3 generated by the LNA can be canceled without affecting the gain and the NF. i_{inj} is expressed as

$$i_{inj} = 2\left(\frac{-3g_1g_3}{4g_2} + \frac{3}{2g_2}\right)A^2\cos(\omega_1 - \omega_2)t \quad (5\text{-}2)$$

It's important to note that, as can be seen from (5-2), if the injected current has a phase φ (≠0), complete IM3 cancellation is impossible. In other words, linearization is degraded with |φ| increasing. However, the phase relationship is not difficult to achieve because the injected signal is located at low-frequency (ω_1-ω_2). Thus this technique is applicable for wide range of systems because the injected signal is not related to the RF frequency but the channel spacing (ω_1-ω_2), and may be used in wideband applications. Furthermore, effective cancellation over wide range of input power may be achieved because the injected signal is tracking the input signal power, as shown in (5-2).

Simple squaring circuit, as shown in Fig. 5.2 is used to generate a voltage proportional to A^2 of the input signal. The squaring circuit input can be directly from the LNA input, or from LNA output if it is in phase or out of phase with the input, the output voltage is applied to M3 and converted to the desired current. PMOS

transistors are used to achieve the negative coefficient g_2 required for cancellation. The simple IM2 injection circuit only consumes an extra current of 0.2mA but suppresses the IM3 by more than 8dB. The AC coupling R2 and C1 set the lower frequency bound of the tone spacing for the linearization to work properly, while R1 and parasitic capacitor from M3 set the upper bound of the tone spacing due to the phase requirement.

All of the noise generated by the squaring circuit is injected at the common source connection of the differential pair. Since this noise appears as a common-mode current, it is rejected by the high common-mode rejection ratio of the differential pair. Gain tuning is realized with current steering pair M4, M6, and M5, M7. M6 and M7 are directly connected to Vdd to avoid distortion contribution at low gain setting. To help reject the image of the 1st down-conversion because of the dual-conversion receiver architecture, inductive load is employed in the LNA, which can also drive large loading capacitor from later mixer stage. Simulation shows the LNA delivers 17dB maximum gain to the mixer, with 9dBm IIP3 and 6dB NF.

The LNA is turned on to enhance the sensitivity in the listen mode, while bypassed to deal with the large self-interferer in the talk mode.

b) Experimental Result

The LNA measure an S11 of better than -15dB from 860MHz to 960MHz as shown in Fig. 5.3. In bypass mode, the LNA has 2dB loss while in normal operation the gain is larger than 15.5dB in the frequency of interest as illustrated in Fig. 5.4. The LNA measures a NF of 6.3dB and 8dB in normal operation and bypass mode respectively

as shown in Fig. 5.5.

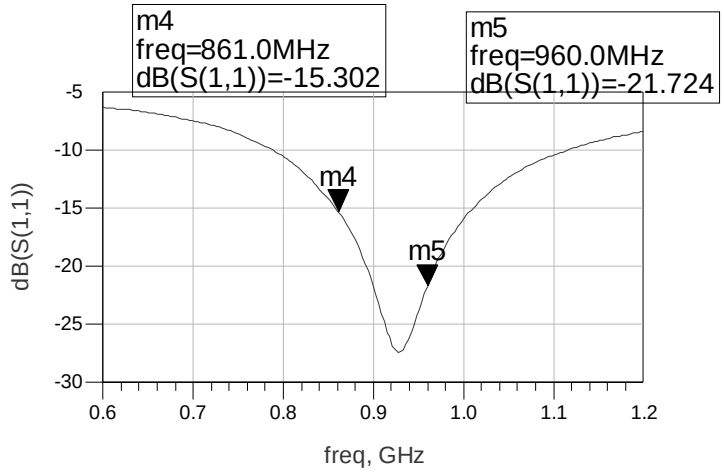
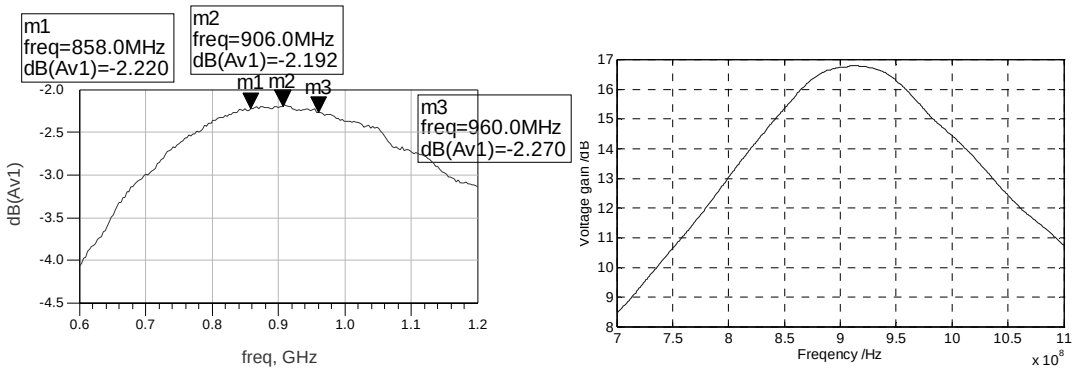
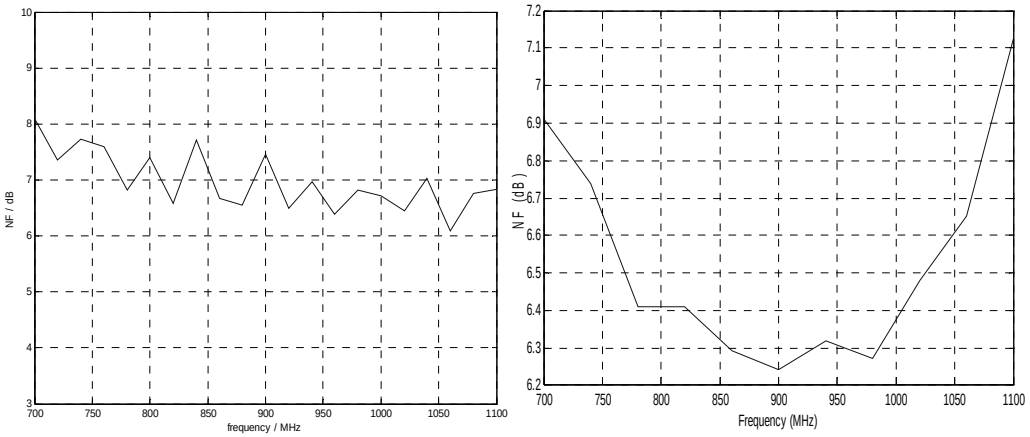


Fig. 5.3 Measured S11 of the LNA



(a) (b)

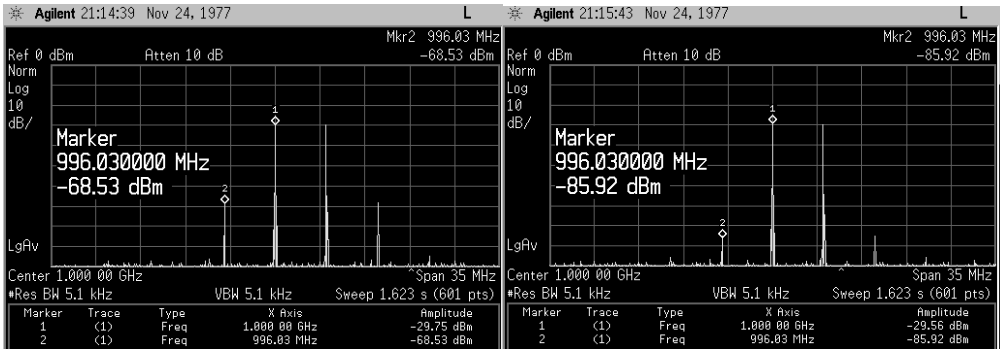
Fig. 5.4 Measured frequency response of LNA (a) bypass mode (b) normal operation



(a) (b)

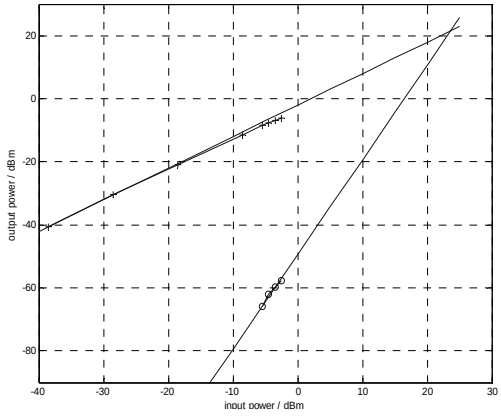
Fig. 5.5 Measured NF of LNA (a) bypass mode (b) normal operation

Fig. 5.6 shows the measured LNA output with two tone inputs, 17dB IM3 suppression is observed after linearization circuits turned on, which demonstrates the effectiveness of this technique. The measured IIP3 of the LNA is illustrated in Fig. 5.7. Table 5.1 summaries the performance of the LNA.

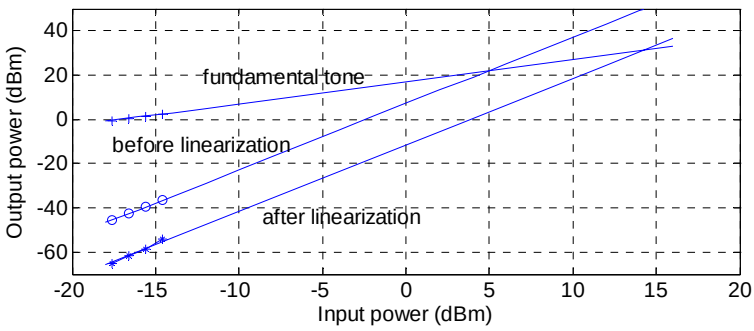


(a) (b)

Fig. 5.6 Measured IM3 at LNA output (a) before linearization (b) after linearization



(a)



(b)

Fig. 5.7 Measured LNA IIP3 (a) bypass mode (b) normal operation

Table 5.1 Performance summary of the LNA

Parameter		Performance
Supply Voltage (V)		1.8
S11 (dB)		<-15
Normal mode	Voltage Gain (dB)	15.4-16.8
	NF (dB)	6.3
	IIP3 (dBm)	8.9
	Input 1-dB Compression Point (dBm)	-4.5
	Power Consumption (mW)	18.7
Bypass mode	Voltage Gain (dB)	-2
	NF (dB)	8
	IIP3 (dBm)	23.6
	Input 1-dB Compression Point (dBm)	5.5

5.2.2 Down-Conversion Mixer

a) Circuit Design

The linearity of the down-conversion mixer is the most critical in the whole receiver chain. In talk mode even with LNA bypassed, it has to tolerate the CW signal as large as 0dBm without saturation. For high linearity, passive mixer is a good option and implemented in [4]. However, the mixer gain would be crucial to suppress the noise in listen mode for the target sensitivity of -90dBm. Even in talk mode, if the front-end virtually has no gain or exhibits loss, it is possible that the thermal noise become comparable or even larger than the noise due to the CW's phase noise, thus further reduces the RX sensitivity. The challenge of the down-mixer is therefore highly linear while still exhibits some gain.

The schematic of the two stage IQ down-conversion mixer is shown in Fig. 5.8. The first mixer employs MOSFET operating in triode region as the input transconductance for good linearity. The first and second stage mixers are interfaced

in current mode by stacking the second stage I and Q mixers on top of the outputs of the first mixer, the signal current is divided into two paths and then mixed with I and Q LO signals. This current mode interfacing technique has much better linearity performance compared to the traditional cascade interfacing in voltage mode. The double converted signal current is then folded with current sources ($M3_{a-d}$ and $R1_{a-d}$) and cascode transistor $M4_{a-d}$. The folded cascode structure increases the output voltage swing and minimizes the signal dependent voltage variation on the drain nodes of $M3_{a-h}$. Finally the down converted signal current is converted into voltage with resistive load.

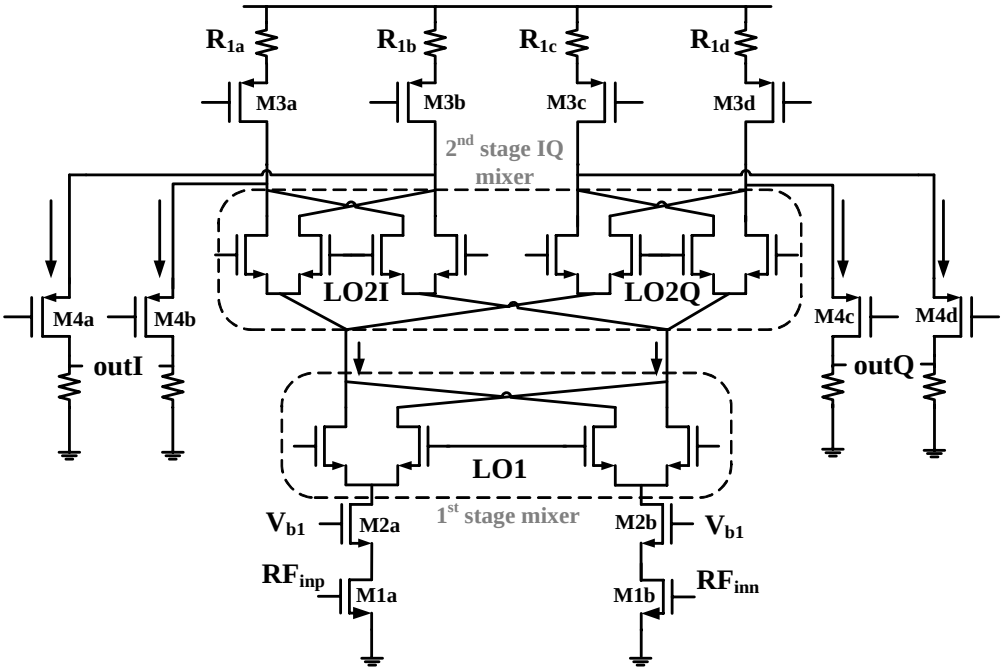


Fig. 5.8 Schematic of the proposed two-stage IQ down-mixer

The sizing and biasing of each transistor is critical in achieving high performance especially for this topology with multiple transistors cascode together. The channel length of the input transistor $M1_{a,b}$ is optimized for maximum linearity and minimum flicker noise without introducing significant capacitive loading to the LNA. As to the

gate bias voltage of $M1_{a,b}$, the output resistance of a triode region transistor is expressed as

$$r_{o1} = \{\frac{\mu C_{ox} W}{L}(v_{GS} - V_{th} - v_{DS})\}^{-1} \quad (5\text{-}3)$$

It is evident that small V_{GS1} is favorable to maximize r_{o1}, but it will lower the V_{dsat} and possible $V_{DS,}$ and hence the gain of the circuit. Moreover, lowering the V_{GS1} limits the -1dB compression point of the circuit as it is limited by the cutoff of M1 [5]. So, V_{GS1} is designed so that it is just large enough for required input referred -1dB compression point and for the required V_{DS1}, or for required DC current of the other cascode devices M2 because V_{GS1} also control the DC current of other cascode devices. Although increasing the W/L ratio of M_2 help stabilizing V_{DS1}, but it cannot be increased too much because of the non-linear current splitting effect between $1/sC_{gs2}$ and $1/g_{m2}$. Optimal operation point is obtained to increase the ratio of g_{m2}/c_{gs2}, therefore minimize the effect of non-linear current splitting between $1/sC_{gs2}$ and $1/g_{m2}$. For the size of LO1 switching pair it is again optimized for minimal current splitting effect between $1/sC_{gs}$ and $1/g_m$, while for the size of LO2 switching pair it is designed to minimize the noise contribution, minimize g_m with acceptable degradation of linearity. The design consideration is different because the RF input of the first mixer is 900MHz and that of second IQ mixers is only 300MHz [6]-[8].

The main reason to use folded output is to increase the output voltage swing so that the -1dB compression point is not limited by the internal nodes, nor by the output nodes. In order to increase the output impedance of the current source so that all the baseband current is delivered to the output, resistive source degeneration is employed.

The resistance $R1_{a-d}$ is maximized to reduce their noise contribution to the circuit while maintains enough voltage headroom for the rest of the circuit.

b) Experimental result

The measured IIP3 of the two-stage mixer is 0dBV. -1dB compression point is -4.5 dBV (~844mVpp). It exhibits 6.8dB gain and 18dB NF while consuming 21.6mW power from a 1.8V supply. The measured linearity performance is shown in Fig. 5.9 and Fig. 5.10. Table 5.2 summarized the performance of the down-mixer.

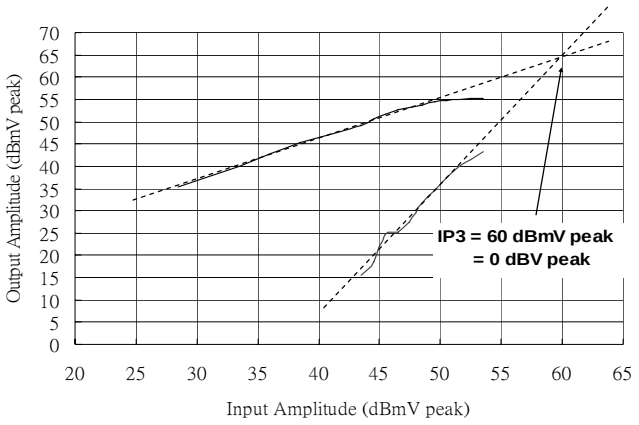


Fig. 5.9 Measured IIP3 of the two stage IQ down-mixer

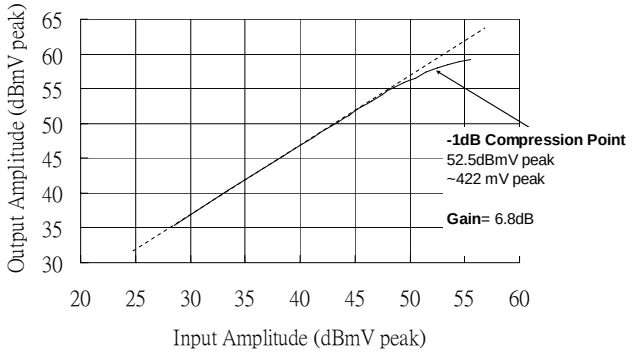


Fig. 5.10 Measured P-1dB of the two stage IQ down-mixer

Table 5.2 Performance summary of the down-mixer

Parameter	Performance
Gain (dB)	6.8
$NF@50\Omega\|_{max\ gain}$ (dB)	18

$IIP3\|_{Min\ gain}$ (dBV)	0
Differential input 1dB compression point rms (dBV)	-4.5
Power (mW)	21.6

5.2.3 A/D Converter

a) Circuit Design

As discussed in section 2.3.3, ΣΔ A/D converter is essential for digital as well as the mixed-mode channel selection. The intrinsic reconfigurablity of the ΣΔ modulator (ΣΔM) makes it a favorable choice for the proposed baseband in that it can trade the resolution in amplitude with the oversampling ratio in time. ΣΔM has been proven to be an effective architecture for the implementation of high resolution (≥12 bits), high bandwidth (≥1MHz) ADC applications [9]-[12]. Specifically, ΣΔM renders inherent high linearity and relieves both the AAF and CSF requirement due to oversampling. The dynamic range (DR) and effective number of bits (ENOB) of ADC is given by

$$DR_{dB} = 10\log[\frac{3}{2}(2^B - 1)(\frac{2L+1}{\pi^{2L}})M^{2L+1}] \quad (5\text{-}4)$$

$$ENOB = \frac{DR_{dB} - 6.02}{1.76} \quad (5\text{-}5)$$

where L is the order of the ΣΔM , M is the oversampling ratio (OSR) of the ΣΔM and B is quantizer's resolution [9]. From (5-4), it can be seen that the DR increases with the above three parameters (L, M, B). Due to stringent linearity requirement, one bit comparator is used. Otherwise, dynamic element matching (DEM) technique such as data weighted averaging (DWA) is necessary to linearize the feedback D/A converter. In Fig. 5.11, the DR of ΣΔM versus OSR M, with different order L is plotted. To meet the target specification, high order is less effective at low OSR, and thus design point of moderate OSR=24 with L=4 has been chosen.

Without the help of multi-bit quantization, single-loop high order design cannot be advantageously implemented due to the instability of high frequency quantization noise particularly at half of the sampling frequency. As a result, MASH 2-1-1 architecture is chosen and implemented using a simple single bit latched-comparator in each stage, which can greatly reduce the complexity and non-idealities such as offset and hysteresis of the comparator contributed to the overall ADC. Yet this architecture with the chosen design point is employed at the expense of relatively high gain amplifier. Particularly for the amplifier in the first integrator, high gain is required for the matching requirement in digital noise cancellation (DNC) and reduction of harmonic distortion and quantization noise leakage. Fortunately, owing to nice noise shaping properties of the modulator, subsequent integrators can be scaled down aggressively. Capacitive loading of subsequent stage and OTA requirement are relieved, and power consumption is reduced.

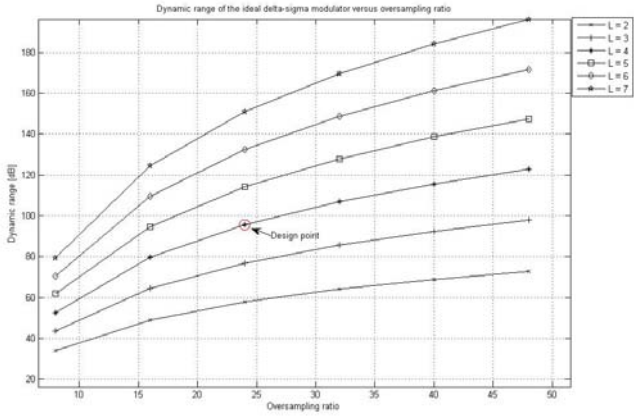


Fig. 5.11 Calculated dynamic range vs. oversampling ratio

There are two architectures suitable for this ADC architecture: cascade of integrators with feedback (CIFB), and cascade of integrators with feedforward (CIFF) [13],[14]. The CIFF architecture is superior in terms of wideband, low distortion and the ease

of MASH implementation. However, it suffers from timing constraint and quantizer overload level reduction [15]. Therefore, the CIFB architecture is extracted. The proposed block diagram of the ADC is depicted in Fig. 5.12.

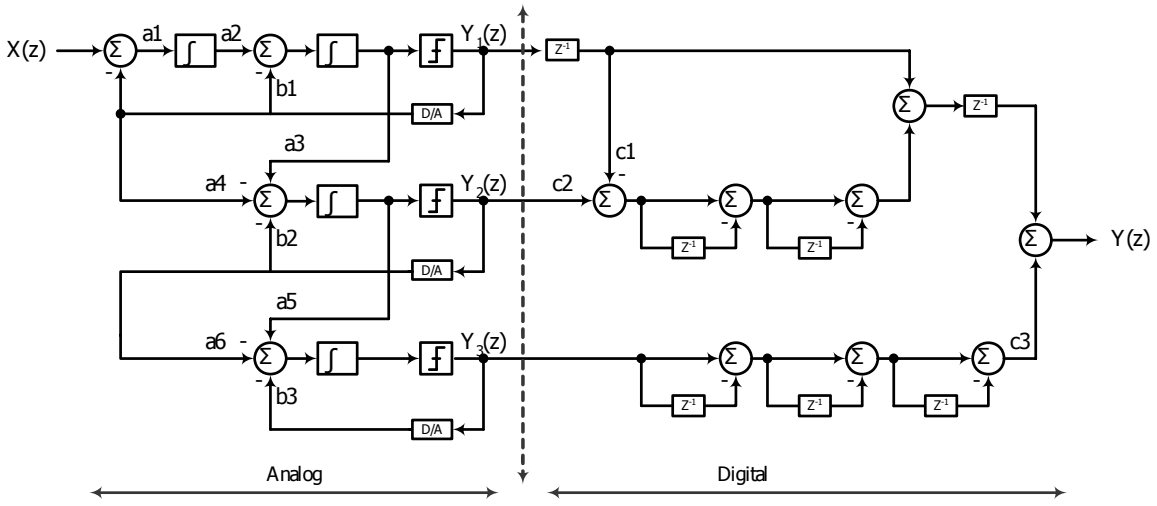


Fig. 5.12 Block diagram of the proposed ΣΔM

The coefficients of the analog and digital part of the proposed ΔΣM are chosen are based on [9], [10] and given by

Analog: [a1 a2 a3 a4 a5 a6 b1 b2 b3]= [1/4 1/2 1 1/4 1 1/4 1/4 1/4 1/4] (5-6)

Digital: [c1 c2 c3] = [-1 2 2] (5-7)

The primarily consideration for selecting the analog coefficient values is the output swing, settling requirement (slew rate and unity gain bandwidth) and in-band noise contribution of each OTA. While for digital part, it is constrained by complexity, power, in-band noise and ease of implementation. Thus, it is purposed to use ±1, 0 or ±2 such that simple wire routing can be served as multiplication and it is worth mentioning that c3 has to be small in order to avoid raised in-band noise floor.

With this coefficient set, the normalized output swing of each integrator versus the normalized input signal level is depicted in Fig. 5.13. At overload level (-3.5dBr), all

integrator attains the maximum swing which is about $0.8V_{pp}$ for 1st and 2nd integrator and $1V_{pp}$ for 3rd and 4th integrator. Using the behavioral model proposed in [16],[17] and the designed ΣΔM parameters are summarized in Table 5.3.

Table 5.3 Summary of specifications of the proposed sigma-delta modulator

Parameters	Specifications
Oversampling ratio	24 or 16
Reference Voltage	1 V
Clock Frequency	40.96 MHz (OSR=16) 61.44 MHz (OSR=24)
Clock jitter	< 500 ps
Switch on resistance	< 150 Ω
DC Gain OTA1 (1st and 2nd) DC Gain OTA2 (3rd and 4th)	> 80dB (worst case) > 53dB (worst case)
Input referred 1st and 2nd OTA noise Input referred 3rd and 4th OTA noise	6 nV $Hz^{-1/2}$ 50 nV $Hz^{-1/2}$
Unity Gain bandwidth OTA1/OTA2 (1.75 pF / 1.75 pF)	> 300 MHz
Slew Rate OTA1 (1.75 pF) Slew Rate OTA2 (1.75 pF)	> 400 V/us > 200 V/us
Differential output swing	> ±1 V
Comparator offset	< ±10 mV
Comparator Hysteresis	< 20 mV

At OSR of 24 and 16, the simulated peak signal to noise and distortion ratio (SNDR) is 79dB and 69dB respectively, while the DR is 84dB and 70dB.

Fig. 5.13 shows schematic of the folded cascode OTA applied in first stage. To further suppress both the quantization noise leakage and the harmonic distortion, the gain boosting techniques are introduced to enhance the DC gain to 80dB while it is still with sufficient output voltage headroom to accommodate the full scale reference. To further increase the matching in two output branches, the differential gain boosted op-amp is chosen to be implemented and therefore an extra continuous time common-mode feedback is embedded. In the subsequent two stages, the gain boosted

op-amps are withdrawn in their OTAs since the noise contributions are greatly suppressed in the ΔΣ loop. In addition, the capacitors could be scaled down to reduce the settling time requirement and hence power.

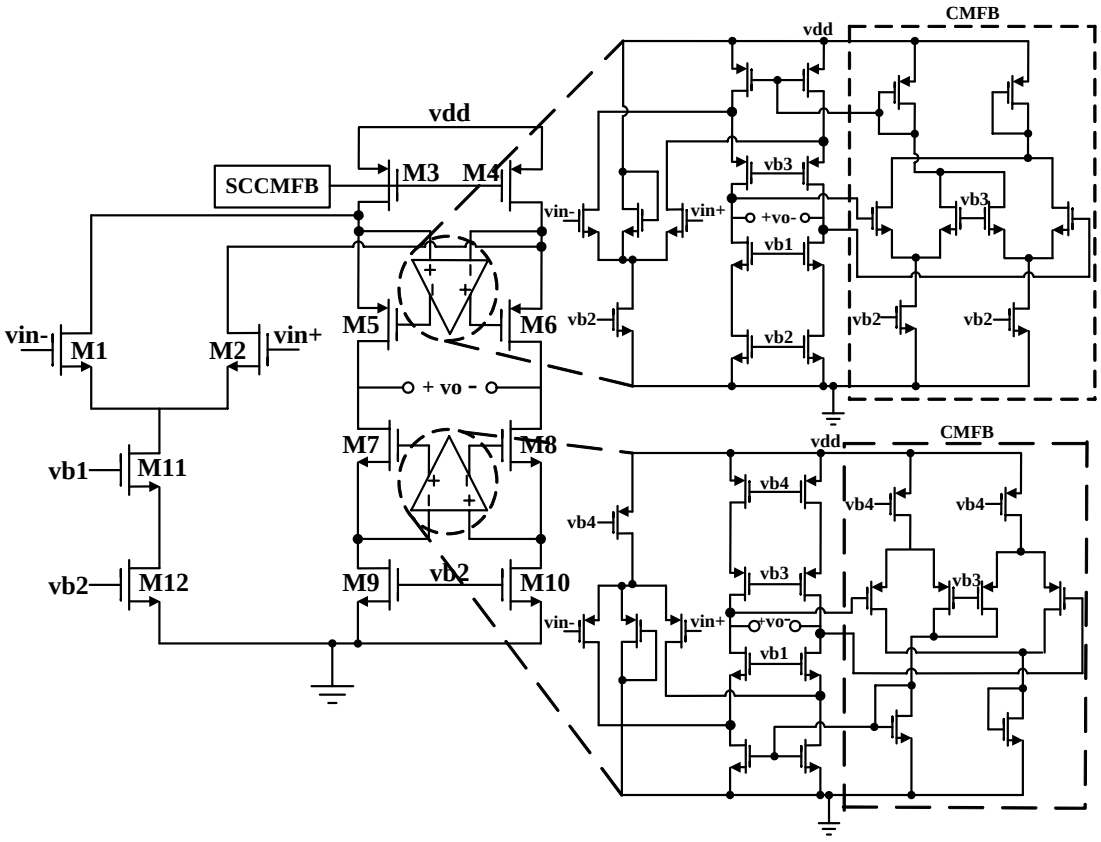


Fig. 5.13 Schematic of the OTAs in the 1st stage

b) Experimental Result

The measured output spectrum with a sinusoid input of -7.8dBFS at 120kHz being sampled at 61.44MHz and baseband bandwidth of 1.28MHz is shown in Fig. 5.14. The measured peak SNR and SNDR are 70.6dB and 68.6dB respectively. To demonstrate the reconfigurability, as the baseband bandwidth changes from 80kHz to 1.28MHz, three cases are selected that are 200kHz, 640kHz and 1.28MHz. Fig. 5.15 depicts the measured SNR and SNDR versus input signal level plot at M = 16 (low DR scenario) and M = 24 (high DR scenario) for all three cases. The measured

dynamic ranges at M = 16 and M = 24 are 67dB and 72dB respectively in all cases. The measured performance of all three cases is summarized in Table 5.4.

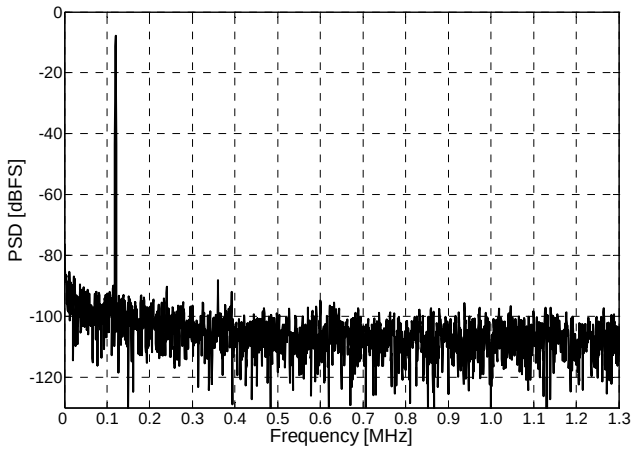


Fig. 5.14 Measured output spectrum at BW=1.28M and OSR=24

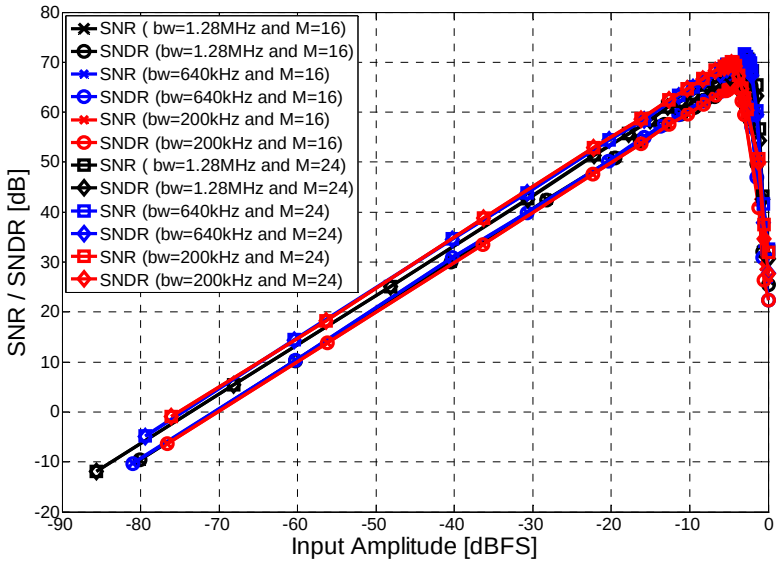


Fig. 5.15 Measured SNR / SNDR versus input level at different BW and OSR

Table 5.4 Performance summary of proposed sigma-delta modulator

Bit rate (kbps)	100		320		640	
Bandwidth (MHz)	0.03 – 0.2		0.096 – 0.64		0.192 – 1.28	
DOR (MS/s)	0.4		1.28		2.56	
Oversampling Ratio	16	24	16	24	16	24
Peak SNR (dB)	65.1	70.1	66.3	71.6	66.4	70.6
Peak SNDR (dB)	65	69.8	65.7	69.5	65.9	68.6
DR (dB)	67	72	67	72	67	72
Power Consumption IQ (mW)	7.4	8.2	16.9	22.4	29.9	39.8

Reference voltage (diff.)	$2V_{pp}$
Supply voltage	1.8V
Technology	TSMC 0.18μm 1P6M CMOS
Core area IQ	$2.96mm^2$

5.3 Transmitter Building Blocks

5.3.1 D/A Converter

a) Circuit Design

Baseband algorithm shows an eight-bit D/A converter is more than enough for RFID application with the sampling frequency less than 5MHz. Among all the architectures, current-steering DAC architecture is the most suitable for moderate resolution, since it can be designed in a standard CMOS technology with evident advantages of cost and power consumption. Current-steering DAC is based on an array of matched current sources that are switched to the output. The difficulty to meet the requirement is due to the random mismatches between the current sources [18].

There are three different architectures available depending on the implementation of the current array, namely binary-weighted, thermometer, and segmented. In general, binary-weighted DACs usually introduce larger glitch energy, which results in larger distortion and intermodulation. On the other hand, thermometer DACs usually provide better performance at the expense of complexity of decoding logic and significant increase of chip area. As a compromise, most current-steering D/A converters are implemented using segmented architecture [18]-[20].

Fig. 5.16 shows the system block diagram of the proposed segmented DAC, which consists of two parts. The 5 MSBs are implemented using the thermometer architecture while the 3 LSBs are implemented with the binary-weighted architecture.

Two-dimensional centroid switching sequence, similar to the one described in [18], is implemented. By simultaneously selecting a symmetrically located current source in each of the four quadrants of the matrix, the systematic error is minimized. A two-stage row-column decoding logic is implemented for the 5-MSBs, which only require NAND and NOR gates with three or two inputs. The 5 input bit streams are decoded into 32-bit thermometer control signals.

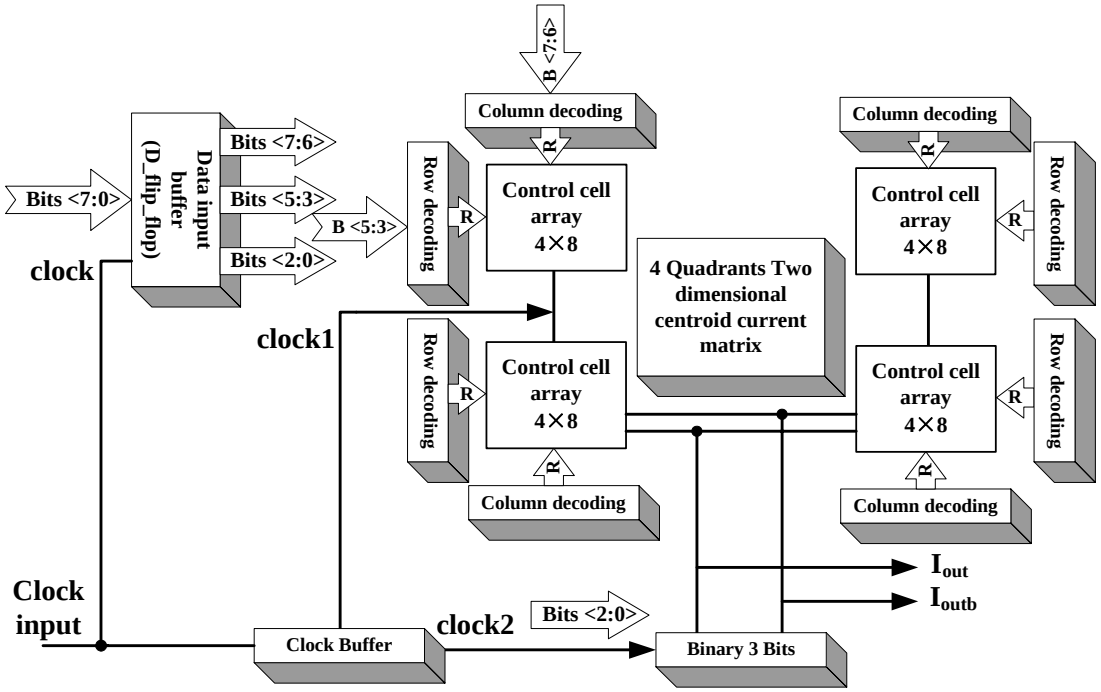


Fig. 5.16 Block diagram of the D/A converter

The schematic of the current cells is shown in Fig. 5.17, which consists of cascode current mirror transistors M1 and M2 to enhance the output impedance for high linearity, switch transistors M3 and M4, and dummy transistors M5 and M6 to minimize clock feedthrough and charge injection.

In order to achieve the best matching results, the switching transistor and cascode transistors are placed in a separate region from the current source transistors. Further, the current source transistors are located in the center of the layout, and to avoid edge

effects, two dummy rows and columns have been added to surround the current source transistors array. In addition, all the current cell transistors are built in deep N-Well, which is available in TSMC 0.18μm CMOS process, to minimize the noise coupling from the substrate. The clock lines and the output lines are designed carefully to minimize the coupling between the digital signals and the analog output signals. The clock lines are distributed by several stages with a tree-structure network to ensure that all the clock signals have the same delay. Lots of attention has been paid to the final layout, resulting in a very compact layout with the area of 1mm×1.6mm for both Q and I channels.

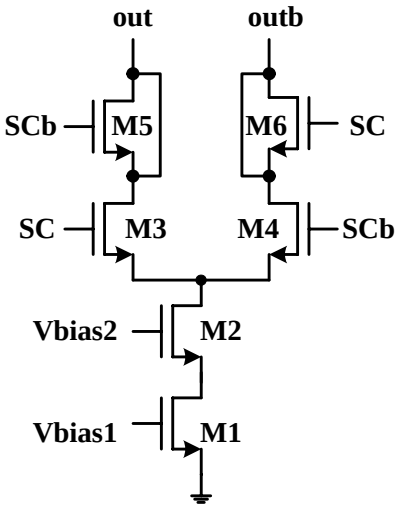


Fig. 5.17 Schematic of the current cell

b) Experimental Result

Sampled at a 5-MSamples/s clock rate, the DAC measures a SFDR of better than 67 dB. Fig. 5.18 shows the output spectrum. Two-tone test result is illustrated in Fig. 5.19, sampled at 5-MSamples/s the SFDR is larger than 60dB. Table 5.5 summarizes the measured DAC performance.

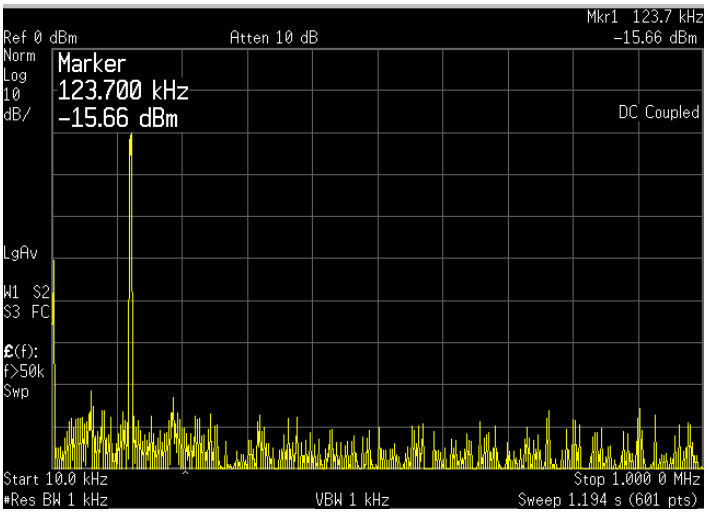


Fig. 5.18 Output spectrum of D/A converter (single-tone input)

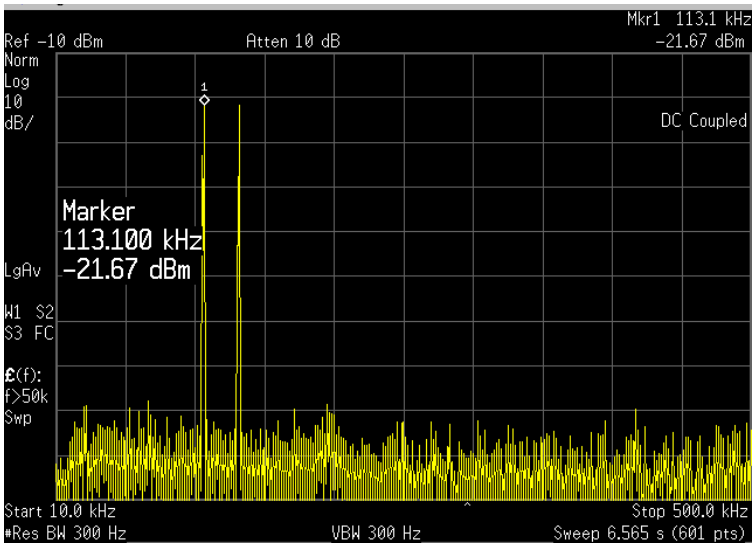


Fig. 5.19 Output spectrum of D/A converter (two-tone input)

Table 5.5 Performance summary of DAC

Parameter	Measurement results
Resolution	8 bits
Supply	1V
Full scale current	1.5mA
DNL	<0.48LSB
INL	<0.45LSB
SFDR	>67dB @ 5MHz
Power consumption (one channel)	2mW
Chip area	1.6×1mm^2 (I&Q channel)

5.3.2 Up-Conversion Mixer

a) Circuit Design

Unlike in down mixer, where the noise, gain and linearity are all crucial to the RX performance, the main concern in up-mixer design is linearity since the TX utilizes ASK modulation scheme. Linearization techniques similar to down mixer design are used, such as MOSFET operating in linear region and techniques to reduce the effect of non-linear current splitting. Current mode interfacing between the 2nd and the 1st mixers is employed to improve linearity.

As shown in Fig. 5.20, the current mode interface between the 2nd and the 1st mixers is implemented with C_{C1} and C_{C2} which couple the sum of up-converted in-phase and quadrature signal current (i_{IFI}+ i_{IFQ} @300MHz) to a low impedance node ($1/g_m$). By doing so, the current is not converted into voltage by a possible nonlinear loading then back to current again by a nonlinear tranconductance, thus high linearity can be maintained. C_{C1} and C_{C2} not only couple the signal current but also isolate the DC voltages between two mixers.

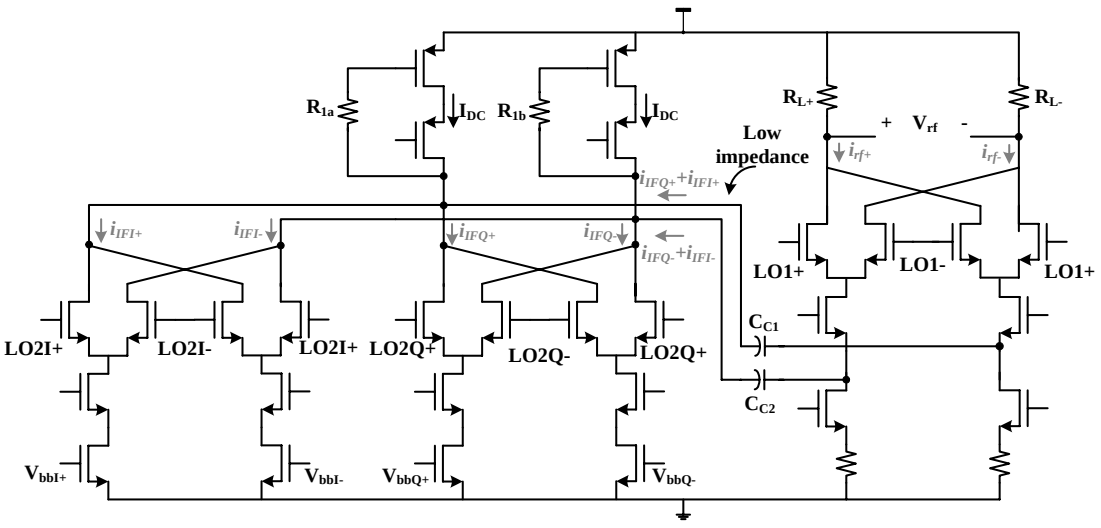


Fig. 5.20 Schematic of the up-mixer

b) Experimental Result

The upmixer measures a gain of -6dB and an input referred 1dB compression point of -12dBV as shown in Fig. 5.21. The IIP3 is 59dBmV which is about -1dBV as illustrated in Fig. 5.22. The measure performance is summarized in table 5.6.

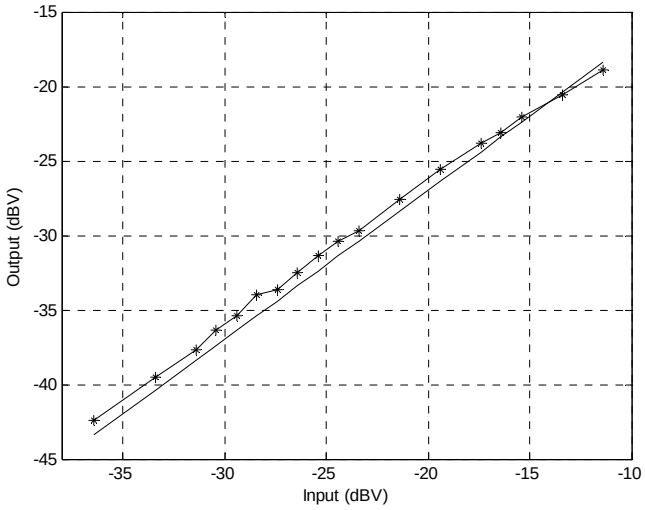


Fig. 5.21 Measured up-mixer P-1dB

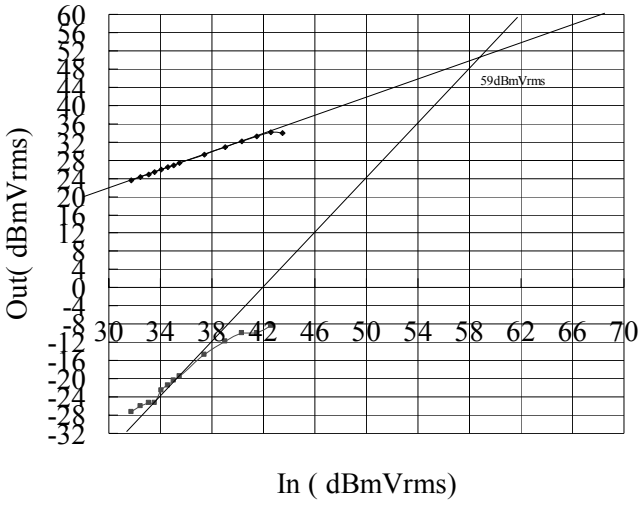


Fig. 5.22 Measured up-mixer IIP3

Table 5.6 Performance summary of the up-mixer

Parameter	Performance
Gain	-6
Input referred 1dB compression point	-12dBV
IIP3	-1dBV
Power	16mA

5.3.3 RF Variable Gain Amplifier

a) Circuit Design

The task of the on-chip RF VGA is to amplify the signal to certain level which is enough to drive the external power amplifier (PA) and provides 20dB tunable gain while exhibits satisfactory linearity. A class-A two-stage folded cascode RF-VGA is designed as shown in Fig. 5.23. High linearity is required due to the system's none constant envelope modulation (ASK) [21]. In order to achieve acceptable efficiency, the output 1dB-compression point of the RF-VGA is chosen to be around 13dBm, which can directly drive TX Antenna for short distance application, or to drive a linear external PA to achieve 1W output power for long distance application.

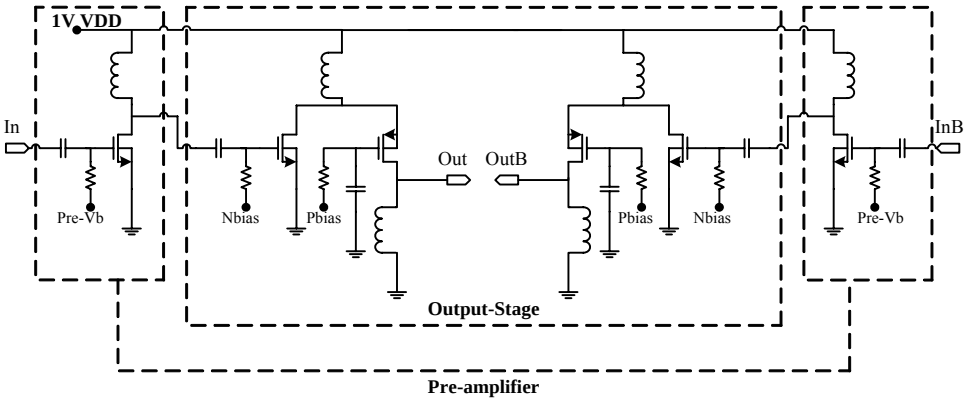


Fig. 5.23 Schematic of the RF-VGA

Depicted in Fig. 5.23, there are in total three center-tap differential inductors integrated on chip to save chip area and enhance Q-factor. Folded cascode structure is implemented in the RF-VGA's output stage, which is able to achieve better linearity when operate under 1V voltage supply, and enhance the stability at the same time [22]. 20dB output power tuning range is implemented by turning on and off pre-amplifier and output-stage's unit cells.

b) Experimental Result

The RF-VGA achieves an output referred 1dB compression point of 11.9dBm and power added efficiency (PAE) of 17%. The maximum PAE is 35% at output power of 15.8dBm. Fig. 5.24 shows the measured output referred 1dB compression point and power efficiency versus the input power. As illustrated in Fig. 5.25, for a fixed input power, the output power can be tuned by larger than 20dB. The two tone test is depicted in Fig. 5.26, the output IIP3 is measured to be 23dBm. The RF-VGA exhibits a bandwidth from 850MHz to 960MHz with peak gain occurred at about 900MHz. At maximum output power, the RF-VGA consumes 122mW from 1V supply. Table 5.7 summarizes the measured performance of the RF-VGA.

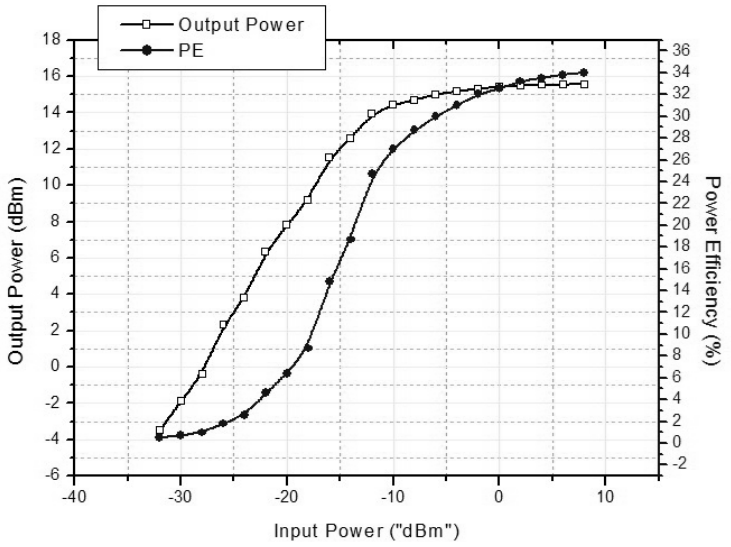


Fig. 5.24 Measured output power and power efficiency versus the input power

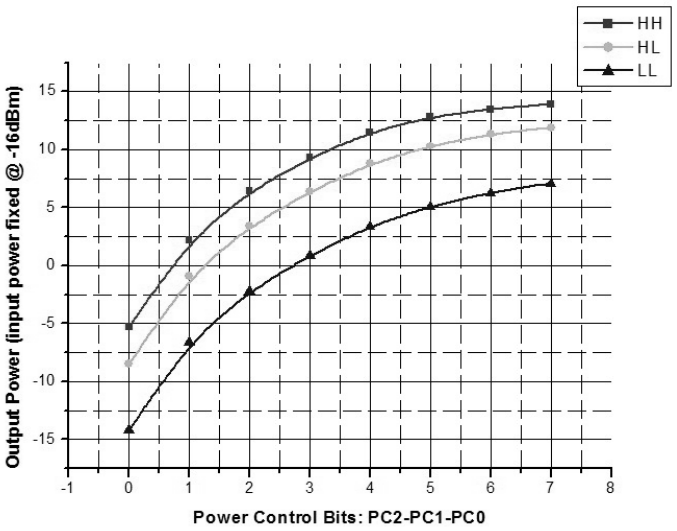


Fig. 5.25 Gain tuning characteristic of the RF-VGA

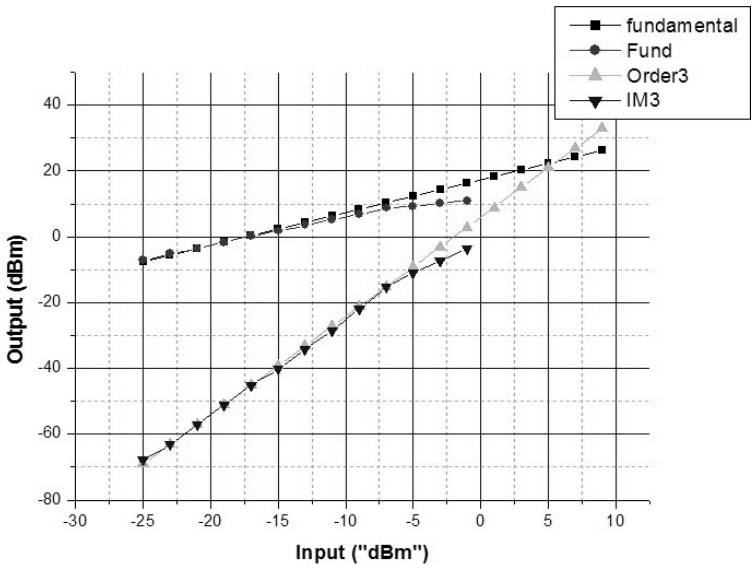


Fig. 5.26 Two tone measurement of the RF-VGA

Table 5.7 Performance summary of the RF-VGA

Parameter	Performance
Small signal gain	19dB
Output P-1 dB	11.9dBm
OIP3	23dBm
PE (~PAE) @ P-1dB	17%
Max PE (~PAE)	35%@15.8dBm
$Power\|_{max}$	122mW

5.4 Reader Digital Baseband

5.4.1 Decimation Filter

After A/D converter, the received signal is in digital format for further signal processing. As shown in Fig. 5.1, the RX baseband portion consists of three main parts: digital decimation filter, automatic gain control (AGC) and front-end processor. In mixed-signal or digital channel selection approach, a decimation filter is required after the oversampled ΣΔ A/D converter to remove both the shaped noise and out-of-band interference. Since the output sampling frequency of the ΣΔ A/D is 16x4 or 24x4 times of the tag-to-reader link-frequency (LF), depending on the OSR. Decimation to four times of LF is needed for synchronization and decoding process in the baseband. The decimation filter is participated into two stages: a comb filter (also known as sinc^k filter) and a 20^{th}-order lowpass finite impulse response (FIR) filter. The comb filter is always chosen as the initial stage of decimation filter for oversampled ΔΣM [23]. It is actually a combining of N integrator stages and differentiator stages. The transfer function of the comb filter is given by

$$H(z) = \left(\frac{1 - z^{-M_C}}{M_C(1 - z^{-1})} \right)^k \tag{5-8}$$

It can be rewritten as

$$H(z) = \left(\frac{1}{M_C} \right)^k (1 - z^{-M_C})^k \left(\frac{1}{1 - z^{-1}} \right)^k \tag{5-9}$$

The filter performs decimation by M_C, which is reconfigurable to either 4 or 6 in this architecture. The order of filter k is given by $k=L+1$, where L is the order of the ΣΔM which is equal to 4 in this design. As in [23], null in magnitude response exists at f_{in}/M_C, where f_{in} is the sampling frequency at the filter input. The architecture of the

comb filter is shown in Fig. 5.27.

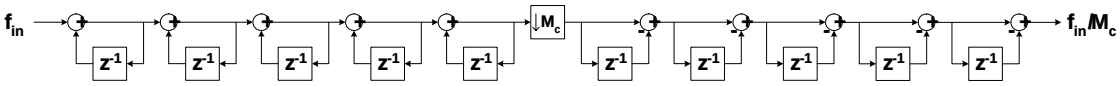


Fig. 5.27 Structure of a five stage comb filter with downsampling ratio equal to M_c

(The normalization operator of $(1/ M_c)^5$ after the differentiators is not shown.)

It is an alternative implementation of (5-9) such that the differentiator is put after the downsampler to reduce the number of delay elements. The register width of the filter needed in preventing the integrators from overflow is given by

$$B_{reg} = k \cdot \log_2(M_C) + B_{in} \tag{5-10}$$

where B_{in} is the input bitwidth from the ΣΔM output.

The comb filter is a good choice because it does not need any multiplier as well as storage for unity coefficients. Thus less silicon area and power is needed. Yet a second stage of decimation filter is required to provide enough attenuation to the shaped quantization noise and adjacent channel interference. The downsampling ratio of this second stage lowpass FIR filter is M_{FIR} = 4. The stopband frequency is four times of the LF i.e. $f_{in\_FIR}/4$ and the achievable stopband attenuation is about 30 dB. Filter coefficients are generated by the Filter Design Toolbox of MATLAB® and quantized to optimal traded between the ideal response and number of bits per coefficients. FIR filter is a better choice than infinite-impulse response (IIR) filter, because its magnitude response can be shaped easily to the desired one with a linear phase response. And the response is less sensitive to quantization error of filter coefficients even for a relatively high order filter. This characteristic can allow shorter coefficient bitwidths and thus smaller circuit size [24]. The architecture of the

filter is shown in Fig. 5.28.

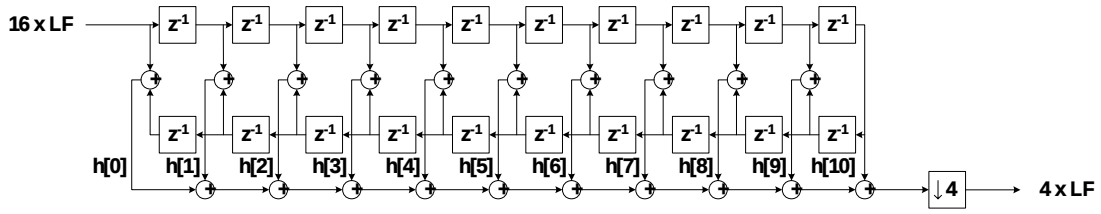


Fig. 5.28 Structure of the FIR filter used for the 2nd stage decimation (Half of the multipliers are needed due to the symmetric nature of FIR filter.)

Simulation of processing a 100 kHz sine wave with the ΣΔM running at OSR=16 along with the decimation filter has been performed. Fig. 5.29 illustrates the time-domain waveform at the outputs of the two filter stages. It is seen that the decimation filter cuts away most of the quantization noise spectrum at the out-of-band frequency range and recovers the sine wave.

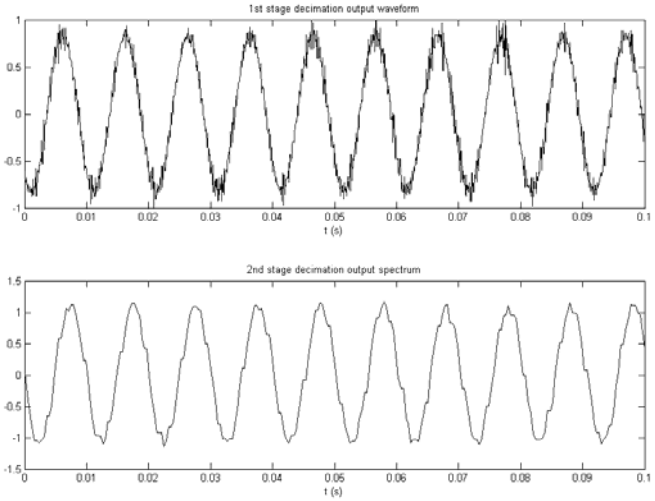


Fig. 5.29 Time domain waveform of different stages the decimation outputs: (upper) First stage comb filter; (lower) Second stage FIR filter

5.4.2 RX Automatic Gain Control

Because of the amplitude variations in the received signal, the A/D converter needs to support a dynamic range of amplification. To remedy this issue, an automatic gain

control is required which keeps the received signal power constant in the dynamic range of the A/D converter. The variable gain in the RF RX chains is distributed among LNA, AAF and CSF, so the critical parameter that AGC needs are gain control step size (resolution = 1dB), conditions of bypassing the LNA, settling time, power reference value P_{ref} as well as the gain control range of each VGA block. Depicted in Fig 5.30, the AGC obtains inputs after the digital decimation filter, and generate gain control bits for LNA, AAF and CSF respectively. The architecture of the AGC is shown in Fig. 5.31. The task of the controller is to control the two chains of VGAs so that the estimated power is as close to a preferred value P_{ref} as possible. An averaged power of 4 samples is first estimated, then low pass filtered and fed through a log function. The control error (E_R) between received signal strength and the power reference value P_{ref} is then formed and fed to a linear control loop which calculates a new gain for the analog VGAs in the RX.

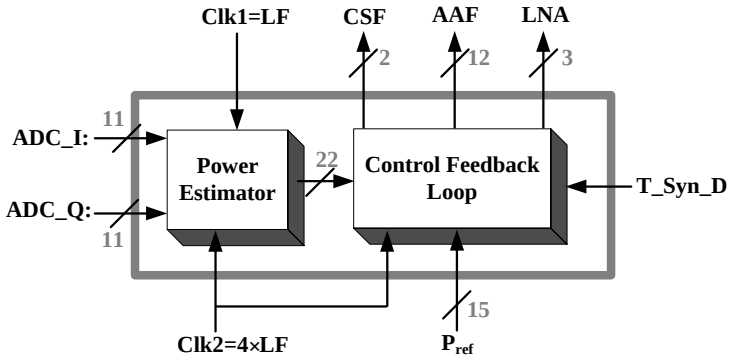


Fig. 5.30 AGC block diagram

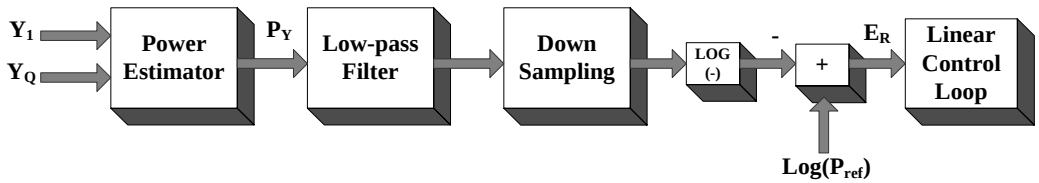


Fig. 5.31 Architecture of the AGC

As illustrated in Fig. 5.32, for an E_R of 1.6dB and settling time within 9 data in the preamble, the convergence error is less than 10^{-3}.

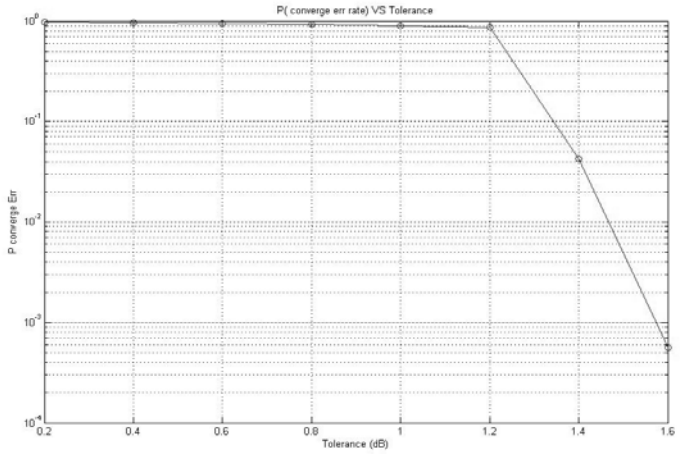


Fig. 5.32 Simulated convergence error rate vs. error tolerance

The detailed physical implementation of the AGC, including an accumulator, a Log Unit and a Feedback Loop is shown in Fig. 5.33. The accumulator performs multiplication, addition and shift operations. This log unit architecture is modified from [25], which performs an approximation of *log2(N)* with *K+M* where *K* is the location of the leading one digit position and *M* is the approximation of *log2(1+M)*. The Feedback loop consists of delay unit and a look-up-table (LUT). The simulated power consumption of the AGC unit is 1.992uW.

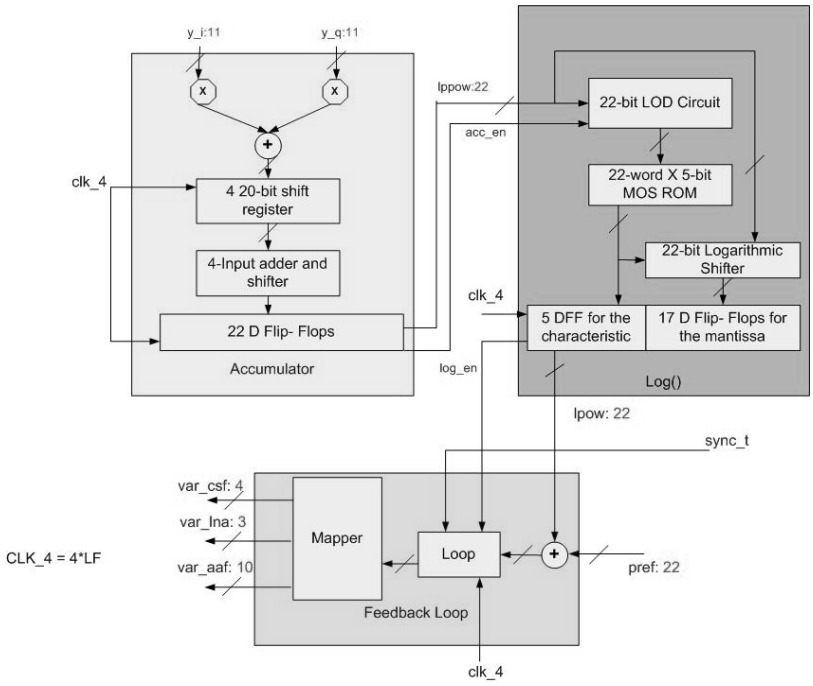


Fig. 5.33 Detailed architecture of the AGC

5.4.3 Reader TX and RX Baseband

As shown in Fig. 5.1, the transmitter of the reader baseband digital portion consists of a CRC encoder, a PIE encoder, and an interpolator. As a command is going to be transmitted, it will first pad with a CRC-5/-16 pattern at its end according to the requirement by the specification. Then the packet is PIE encoded using one of the three Tari values which is decided by the controller. A preamble or frame-sync pattern is put at the beginning of the encoded packet. Finally this PIE encoded packet is 4x upsampled with respect to the period of Tari/4 and interpolated by a raised-cosine filter to obtain a transmitted spectrum within the ETSI mask. This pulse-shaped packet is then converted to analog signal by the 8 bits D/A converter for further processing in analog domain. Fig. 5.34 shows the simulated time domain waveform of the original PIE encoded signal, upsampled PIE signal and final output to the D/A. The TX output spectrum is illustrated in Fig. 5.35 which can fulfills the

EPC Gen-2 dense reader mode spectrum mask.

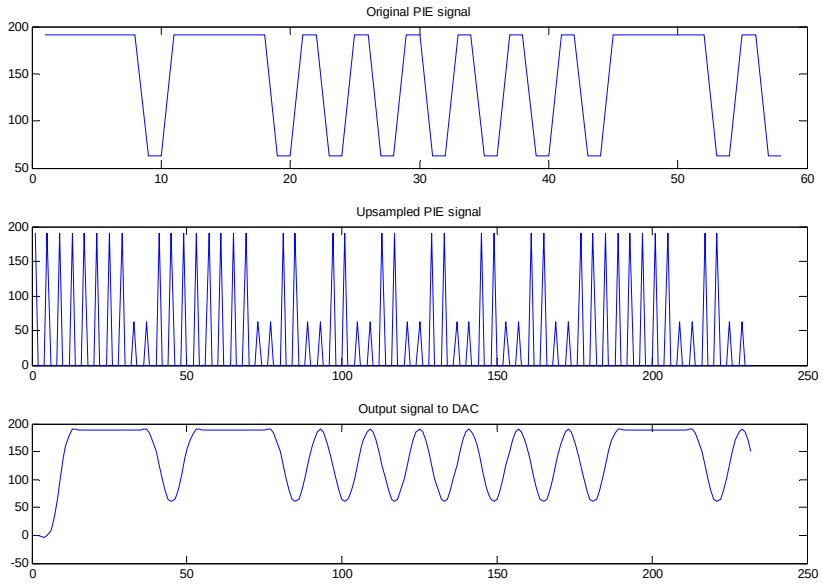


Fig. 5.34 Simulated TX time domain waveform

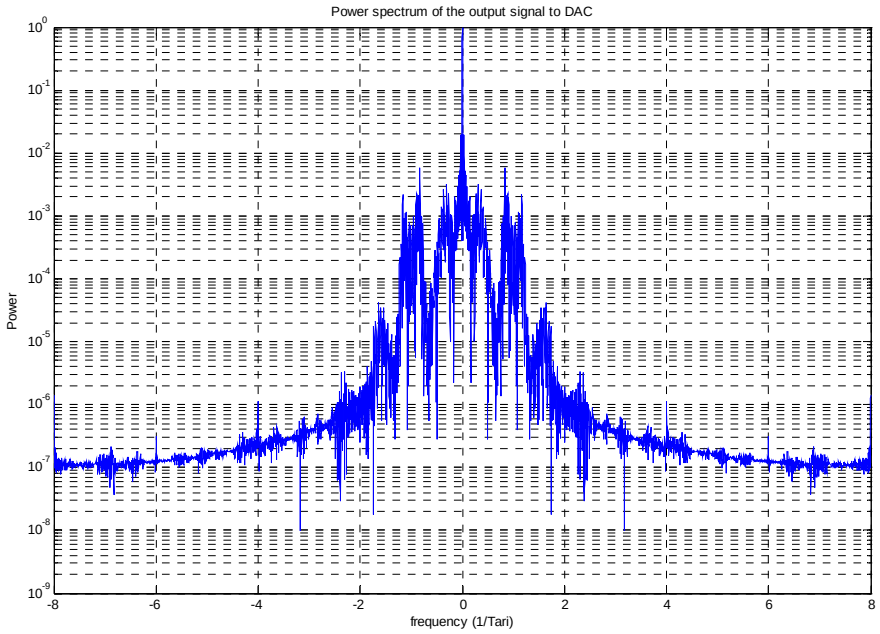


Fig. 5.35 Simulated TX baseband output spectrum

For the RX baseband, as shown in Fig. 5.1 the frontend processor is responsible for detecting the bit boundary (timing synchronization) and start of the packet (frame synchronization) in the backscattered reply from a tag and recovering FM0 or Miller-subcarrier encoded bits. As the modulation scheme used in the tag transmitter

is ASK or PSK, no dedicated baseband demodulator is need and the matched filter in the synchronization and bit decoding processing can do the job. The two synchronizations use running windows to calculate the correlated value in the preamble frame. If the correlated value is bigger than a certain threshold, the bit/frame boundary is found. For bit decoding, the correlated value compared with the threshold value is used to determine if a bit-0 or bit-1 is received. Illustrated in Fig. 5.36, the algorithm employed can achieve bit error rate (BER) equal to 10^{-3} at signal-to-noise ratio (SNR) at about 11dB for ASK FM0 and 9dB for ASK Miller subcarrier with M being 2. PSK modulation has 3dB gain, so the minimum SNR_{out} for PSK is 8dB for FM0 and 6dB for Miller subcarrier respectively.

The simulated power consumption of the RX baseband unit without AGC and decimation filter is 8.44mW for data rate of 640kbps and under a 1.8V supply. The simulated maximum power consumption of the TX baseband is 231.7μW.

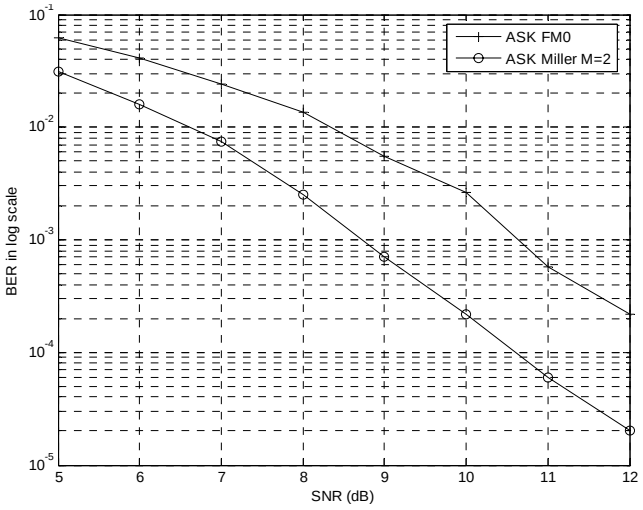


Fig. 5.36 Simulated RX BER vs. SNR for ASK

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Chapter 6
RECONFIGURABLE BASEBAND

6.1 Introduction

As one of the most important features of the multi-protocol reader, the baseband is designed to be highly reconfigurable in terms of architecture, clock frequency, baseband channel bandwidth and power consumption. The goal of this chapter is to provide theoretical foundations and seek a systematic way to optimize power subject to the constraints on circuit performance, e.g. noise, interference and speed. We start with the investigation on the noise in a sampled system, followed by the detailed analysis on the switched-capacitor filter, ΣΔ A/D converter and decimation filter. Finally we apply the obtained model to predict the performance of the entire baseband.

6.2 Noise in a Sampled System

To analyzing the achievable dynamic range of the baseband circuits, it is crucial to understand the features of noise in a sampled system because dynamic range relates to both the maximum signal swing and the circuit noise level which limits the minimum detectable signal.

A simple sample and hold circuit is illustrated in Fig. 6.1. When switch is ON, the output follows the input; when switch is OFF, the voltage sampled in the end of

tracking interval is maintained in the capacitor. Namely the sample process can be viewed as the sum of two functions, one of continuous nature and another of sampled nature.

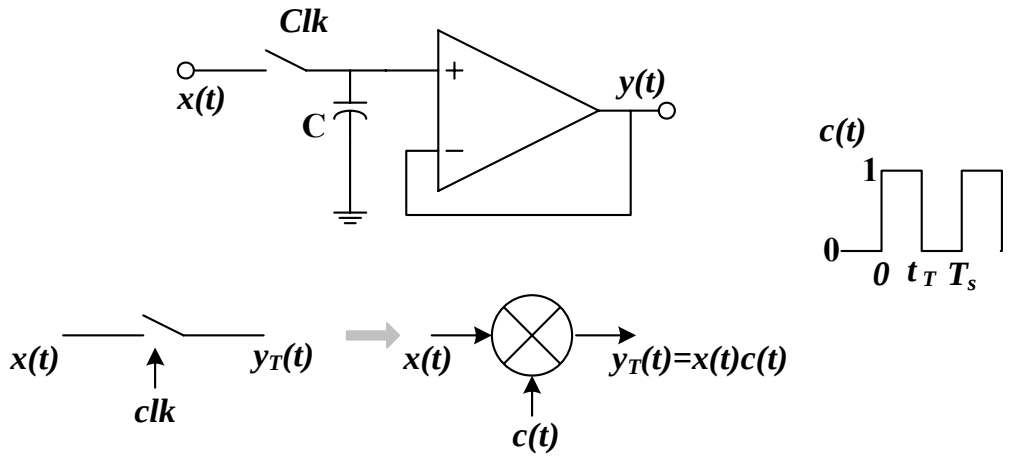


Fig. 6.1 Ideal sample and hold circuit and tracking model

We first look at the noise during tracking operation. Signal *c(t)* is periodic with period T_s and can be expressed as [1]

$$c(t) = \sum_{n=-\infty}^{\infty} \frac{[1-\exp(-jn2\pi f_s \tau_T)]}{j2\pi n} \exp(jn2\pi f_s t) \tag{6-1}$$

Where τ_T is the interval when clock is ON, f_s is sample frequency.

The power spectrum density of the sampled output $y_T(t)$ in Fig. 6.1 is obtained by the convolution product of the two transforms

$$S_{y_T}(f) = S_x(f) \otimes S_c(f) = \left(\frac{\tau_T}{T_S}\right)^2 \sum_{n=-\infty}^{\infty} \sin c^2(n\pi f_s \tau_T) S_x(f - nf_s) \tag{6-2}$$

where

$$\sin c(x) = \begin{cases} 1 & x \equiv 0 \\ \dfrac{\sin(x)}{x} & x \neq 0 \end{cases} \tag{6-3}$$

Assume the *x(t)* is a narrow band noise coming from a white noise being through a

lowpass filter, of which the transfer function is $H_F(f)$ as shown in Fig. 6.2. The noise bandwidth BW_n is defined as the equivalent bandwidth of noise, calculated so that it contains the same power as the represented noise but with constant spectral density S_0, that is [2]

$$S_0 \cdot BW_n = \int_{-\infty}^{\infty} S_0 \left| H_F(f) \right|^2 df \tag{6-4}$$

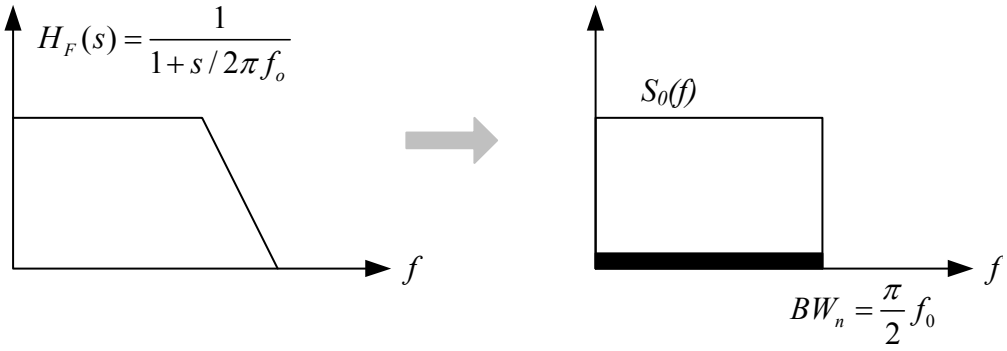


Fig. 6.2 Power spectrum density of a narrow-band noise

If $f_s \geq BW_n$, the spectra centered in integer multiplies of f_s are not overlapped, so no aliasing occurs. On the contrary, if $f_s < BW_n$, it is easy to find out the number of bands that overlapped in the interval $(-f_s/2, f_s/2)$ is BW_n/f_s. Therefore (6-2) can be simplified to

$$S_{y_T}(f) = \begin{cases} \left(\frac{\tau_T}{T_S}\right)^2 S_0 & f_s \geq BW_n \\ \left(\frac{\tau_T}{T_S}\right)^2 S_0 \left[1 + 2 \sum_{n=1}^{BW_n / f_s} \sin c^2 (n\pi f_s \tau_T)\right] & f_s < BW_n \end{cases} \tag{6-5}$$

When $BW_n \geq 5f_s$, (6-5) can be approximated by

$$S_{y_T}(f) = \begin{cases} \left(\frac{\tau_T}{T_S}\right)^2 S_0 & f_s \geq BW_n \\ \frac{\tau_T}{T_S} S_0 & f_s < BW_n \end{cases} \tag{6-6}$$

In sample and hold mode, the output is maintained after switch is OFF. Similar analysis can be applied and the resultant noise is [1]

$$S_y(f)=\begin{cases}\left(\frac{\tau_{SH}}{T_S}\right)^2 S_0\mathrm{sinc}^2(\pi f_s\tau_{SH}) & f_s \geq BW_n \\ \left(\frac{\tau_{SH}}{T_S}\right)^2 S_0\frac{BW_n}{f_s}\mathrm{sinc}^2(\pi f_s\tau_{SH}) & f_s < BW_n\end{cases} \tag{6-7}$$

Assume a non-overlapping clock with two equal phases, that is $\tau_T = \tau_{SH} = T_S/2$. Since the noise is uncorrelated, the total noise is the sum of (6-6) and (6-7)

$$S_y(f)=\begin{cases}\frac{S_0}{4}[\mathrm{sin}\,c^2(\frac{\pi fT_S}{2})+1] & f_S \geq BW_n \\ \frac{S_0}{4}[\frac{BW_n}{f_S}\mathrm{sin}\,c^2(\frac{\pi fT_S}{2})+2] & f_S < BW_n\end{cases} \tag{6-8}$$

The noise folding effects can be graphically viewed in Fig. 6.3, when aliasing is produced, the spectrum density of the sampled noise increases in the band of interest. As a result, it is usually assumed that the full power appears in the frequency band of $-f_s/2$ and $f_s/2$ with an approximately white spectrum density.

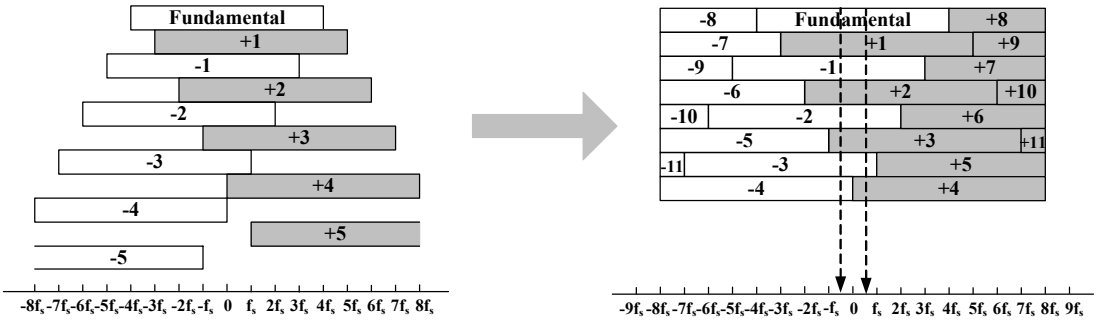


Fig. 6.3 Noise folding when $f_s<BW_n$

The circuit in Fig. 6.4(a) is a simplified schematic of typical sampling network in the switched-capacitor (SC) circuit. When *clk* is high, the sampled noise power can be estimated using the circuit in Fig. 6.4(b), where the MOS switch is modeled as a resistor in series with a noise voltage. If the sampling time is much longer than the

time constant formed by R_{on} and C_s, then the voltage drop across the MOS switch is approximately zero at the end of the sampling phase. So the transistor is in linear region and the noise factor is 1. Furthermore, the switching process resets trapping states at the silicon-oxide interface, thereby preventing the accumulation of low frequency flicker noise. Thus, flicker noise can be neglected in such circuits [3].

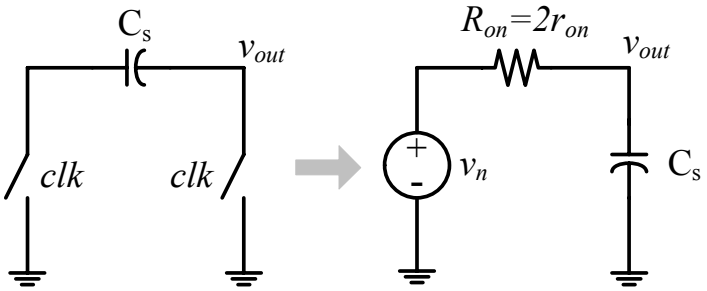


Fig. 6.4 (a) A switched-capacitor sampling network; (b) Model for noise estimation

The thermal noise of the resistor is white and has a one-side power spectral density of

$$\frac{v_N^2}{\Delta f} = 4kTR_s \tag{6-9}$$

Depicted in Fig. 6.4 (b), the broadband resistor noise is being filtered by the single-pole lowpass filter formed by R_{on} and C_s. The total output noise is

$$v_{n,out}^2 = \frac{1}{2\pi}\int_0^\infty |H(j\omega)|^2 v_N^2 d\omega \tag{6-10}$$

where

$$|H(j\omega)|^2 = \frac{1}{1+(\omega R_{on}C_s)^2} \tag{6-11}$$

Substituting (6-9) and (6-11) into (6-10) yields

$$v_{n,out}^2 = \frac{4kTR_{on}}{2\pi}\int_0^{\infty}\frac{1}{1+(\omega R_{on}C_s)^2}d\omega$$
$$= \frac{2kTR_{on}}{\pi}\left(\frac{1}{R_{on}C_s}\right)\arctan(\omega R_{on}C_s)\Big|_{\omega=0}^{\omega=\infty} = \frac{kT}{C_s} \quad (6\text{-}12)$$

Because of the noise folding effect, the noise is uniformly distributed across the Nyquist band. If a frequency of f_s is used to sample the signal of baseband bandwidth f_b, the oversampling ratio (OSR) is defined as

$$M = \frac{f_s}{2f_b} \quad (6\text{-}13)$$

Then the thermal noise power appear in the band of interest is

$$v_{n,in}^2 = \frac{kT}{C_s f_s/2} f_b = \frac{kT}{C_s M} \quad (6\text{-}14)$$

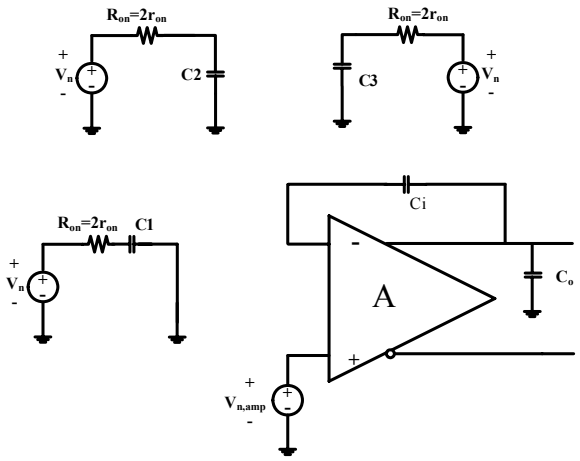
(6-14) forms the fundamental of noise in the sampled circuits and the basis for further analysis in this chapter.

6.3 Power Dissipation of the Channel Selection Filter

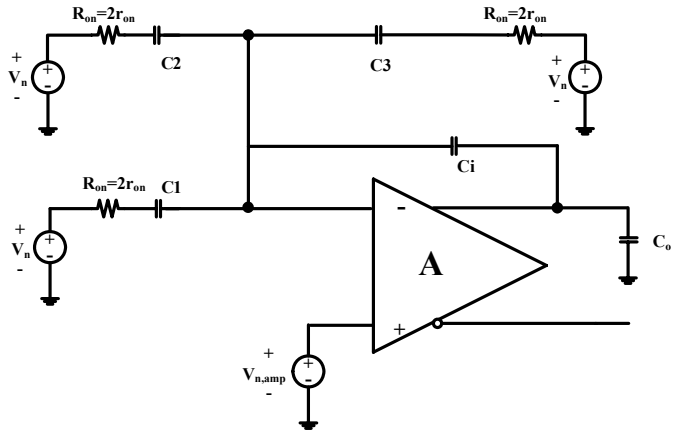
6.3.1 Input-referred Thermal Noise of the 1st-order Lowpass Filter

In the SC circuit, the noise is sampled together with the signal at the sampling capacitor, which is generated not only by the non-zero on resistance of the switches as discussed in previous section, but also by that of the amplifier, On the other hand, the need of minimizing charge transfer errors recommends the use of time constants that are small compared with clock period. This implies a wideband noise being filtered by a lowpass filter with small cutoff frequency; therefore aliasing and noise folding occur. To perform the analysis in the CSF, we will suppose that all sources are of white noise and are not correlated, which permits the application of the

principle of superposition. We further assume the opamp gain is infinite and neglect the influence of finite bandwidth of the opamp on charge transfer and parasitic capacitance. Since the 1st-order lowpass filter dominates the noise in the CSF, we will focus on the investigation of its noise.



(a)



(b)

Fig. 6.5 Model for noise analysis of the 1st-order lowpass filter: (a) sample phase ϕ_1; (b) integration phase ϕ_2

The model for noise analysis of the 1st-order lowpass filter is shown in Fig. 6.5. The speed of the circuit is limited by the bandwidth in both clock phases. Normally the integration phase is the most critical as will be illustrated later. The -3dB bandwidth

is determined by the unity gain frequency of the opamp and the feedback factor. Denote that the feedback factor on ϕ_1 is β_1, while on ϕ_2 is β_2

$$\beta_1 = 1 \tag{6-15}$$

$$\beta_2 = \frac{C_i}{C_1 + C_2 + C_3 + C_i} \tag{6-16}$$

For a single-stage opamp, the unity-gain frequency is

$$\omega_u = \frac{g_m}{C_{load}} \tag{6-17}$$

where g_m is the transconductance of the input transistor. The load capacitance on ϕ_1 is C_{L1}, while on ϕ_2 is C_{L2}

$$C_{L1} = C_i + C_o \tag{6-18}$$

$$C_{L2} = C_o + \beta_2(C_1 + C_2 + C_3) \tag{6-19}$$

where C_o is assumed to be a fixed loading capacitor on both clock phases. Thus the -3dB bandwidth on ϕ_1 is given by

$$\omega_{-3dB,\phi_1} = \beta_1\omega_{u1} = \frac{g_m}{C_i + C_o} \tag{6-20}$$

while on ϕ_2 is

$$\omega_{-3dB,\phi_2} = \beta_2\omega_{u2} = \frac{g_m C_i}{C_i(C_1 + C_2 + C_3) + C_o(C_1 + C_2 + C_3 + C_i)} \tag{6-21}$$

On clock phase 1, the noise voltage from switches stored on the capacitors is

$$v_n^2 = \frac{kT}{C_1 + C_2 + C_3} \tag{6-22}$$

So the total noise charge is

$$q^2 = \sum \frac{kT}{C_i} \cdot C_i^2 = kT(C_1 + C_2 + C_3) \tag{6-23}$$

On clock phase2, the charge will transfer to the output and convert to a voltage

$$v_{n,\phi_1}^2 = \frac{q^2}{C_i^2} = \frac{kT(C_1 + C_2 + C_3)}{C_i^2} \tag{6-24}$$

While for differential circuit, a factor of two is added to account for noise from two branches

$$v_{ndif,\phi_1}^2 = \frac{q^2}{C_i^2} = \frac{2kT(C_1 + C_2 + C_3)}{C_i^2} \tag{6-25}$$

When referred to the input, (6-25) divided by the gain of the circuit results in

$$v_{inn,\phi_1}^2 = v_{ndif,\phi_1}^2 \frac{C_i^2}{C_1^2} = \frac{2kT(C_1 + C_2 + C_3)}{C_1^2} \tag{6-26}$$

Next, we study the opamp noise. The z-domain output noise from the opamp noise source ($v_{n,amp}$) can be derived based on charge conservation [4]. On clock phase ϕ_1 (t=(n-1)T) we have the total charge

$$q_1 = v_o(n-1)C_i - v_{n,amp1}(n-1)C_i - V_o(n-1)C_3 \tag{6-27}$$

Where $v_x(n-1)$ denotes the voltage at time t=(n-1)T, $v_{n,amp1}$ is the noise power due to opamp in ϕ_1. In the next clock phase ϕ_2 (t=(n-1/2)T), the total charge is

$$q_2 = v_o(n-\frac{1}{2})C_i - v_{n,amp2}(n-\frac{1}{2})(C_i + C_1 + C_2 + C_3) \tag{6-28}$$

Where $v_{n,amp2}$ is the noise power due to opamp in ϕ_2. The total charge in the two clock phases is conserved. Therefore $q_1=q_2$, i.e.

$$[v_o(n-1) - v_{n,amp1}(n-1)]C_i - [v_o(n-1) - v_{n,amp2}(n-\frac{1}{2})]C_3 = [v_o(n-\frac{1}{2})C_i - v_{n,amp2}(n-\frac{1}{2})]C_i - v_{n,amp2}(n-\frac{1}{2})(C_1 + C_2) \tag{6-29}$$

There is one additional constraint, in the next clock phase ϕ_1, the output is held by C_i. The total charge on C_i is conserved, i.e.

$$v_o(n-\frac{1}{2})-v_{n,amp2}(n-\frac{1}{2})=v_o(n)-v_{n,amp1}(n) \tag{6-30}$$

Substituting (6-30) into (6-29) and rearranging yields

$$v_o=v_{n,amp1}\frac{C_i(1-Z^{-1})}{(Z^{-1}C_3-Z^{-1}C_i+C_i)}+v_{n,amp2}\frac{Z^{-1/2}(C_1+C_2+C_3)}{(Z^{-1}C_3-Z^{-1}C_i+C_i)} \tag{6-31}$$

Divide the output referred noise by the transfer function of the 1st-order lowpass filter, we obtained the input referred noise

$$v_{n,in}=v_{n,amp1}\frac{i(Z-1)}{Z+1}+v_{n,amp2}\frac{Z^{1/2}(2+a)}{Z+1} \tag{6-32}$$

where we define

$$C_1=C,\ C_2=C_1=C,\ C_3=a\times C,\ C_i=i\times C,\ C_o=n\times C \tag{6-33}$$

It is usually more convenient to express in this way because all the transfer function is given by capacitor ratios in a switched-capacitor circuits. Besides, in the layout, capacitor is also represented in terms of unit capacitors and capacitor ratios to minimize the mismatches and achieve high accuracy.

Note that the first term in (6-32) has a highpass characteristic. If the filter is over-sampled, the second term will dominate. In the proposed system, the CSF has the same clock frequency as the over-sampled A/D, so only the second term is taken into account. Input referred noise due to the opamp noise is thus

$$v_{inn,\phi_2}^2=v_{n,amp2}^2(2+a)^2 \tag{6-34}$$

where the opamp noise in ϕ_2 is

$$v_{n,amp2}^2=2\cdot\frac{8}{3}\frac{kT}{g_m}\cdot(1+n_t)\frac{\beta_2\cdot\omega_{u2}}{4} \tag{6-35}$$

Where n_t is the noise contribution factor due to the other noise sources. It is worth mentioning that the noise source on clock phase 2 is from sampling C1 (v_{n1}),

sampling C2 (v_{n2}), sampling C3 (v_{n3}) and opamp ($v_{n,amp}$). Analysis shows that the ratio of noise due to sampling switches and noise due to opamp is approximately in the order of g_mR_{on} [5]. Because the product of g_mR_{on} is usually 0.1 or less, ignoring the noise contributions of switches generates only 10% of error [1]. Thus only the opamp noise is of concern in ϕ_2. Finally, the total input referred noise is obtained by summing the noise in ϕ_1 and ϕ_2. Substitution of (6-26), (6-34) and (6-35) yields

$$v_{in}^2 = v_{inn,\phi_1}^2 + v_{inn,\phi_2}^2 = \frac{2kT(2+a)}{C}[1+\frac{2}{3}\cdot\frac{i(1+n_t)(2+a)}{n(2+a+i)+i(2+a)}] \tag{6-36}$$

The noise power inside the bandwidth of interest f_b is thus

$$\begin{aligned} v_{tot,in}^2 &= \frac{4kTf_b(2+a)}{f_sC}[1+\frac{2}{3}\cdot\frac{i(1+n_t)(2+a)}{n(2+a+i)+i(2+a)}] \\ &= \frac{2kT(2+a)}{MC}[1+\frac{2}{3}\cdot\frac{i(1+n_t)(2+a)}{n(2+a+i)+i(2+a)}] \end{aligned} \tag{6-37}$$

6.3.2 Power Consumption of the 1st-order Lowpass Filter

To achieve the desired dynamic range under a fixed supply voltage, the circuit noise level has to be properly designed. The noise specification of the filter is obtained from system calculations to meet the overall noise requirement. In such a noise oriented design approach, the most power efficient design is to minimize the power consumption subject to the constraints on noise and settling time.

The worst case driving situation for the opamp occurs in the integration phase as shown in Fig. 6.5(b) and (6-21). As discussed in chapter4, in the proposed CSF current mirror opamp is employed because an opamp with large unity gain bandwidth and slew rate but moderate DC gain is required. The response of an operational amplifier that employs a differential pair as its input stage typically

includes a slew limited region followed by a linear settle region. The duration of the slew limited region is

$$T_{SL} = \frac{V_f}{S} \tag{6-38}$$

where V_f is the asymptotic final value of the output voltage, S is the slew rate. V_f is the output swing of the filter given as

$$V_f = A_v V_{in} \tag{6-39}$$

where A_v is the voltage gain and V_{in} is the input voltage amplitude. Assume 0.1% accuracy has to be achieved, the linear settling time is at least (analysis can be found in 4.4.3)

$$T_{lin} = 7\tau \tag{6-40}$$

where τ is the settling time constant.

Assume the sampling time, i.e. the sum of the duration of the two regions is about 80% of half clk periods

$$\frac{T_s}{2} = (T_{SL} + T_{Lin}) / 0.8 = 1.25(\frac{A_v V_{in}}{S} + 7\tau) \tag{6-41}$$

For the slew rate of current mirror opamp,

$$S = \frac{2I_2}{C_{L2}} = \frac{2KI_1}{C_{L2}} \tag{6-42}$$

Where C_{L2} is the effective loading cap in the integrating phase given by (6-19), I_1 is the drain current of each input transistor, I_2 is the current of each output branch, K is the current ratio of these two branches. τ is defined as

$$\tau = \frac{1}{\omega_{-3dB,\phi_2}} = \frac{C_{L2}}{Kg_{m1}\beta_2} \tag{6-43}$$

Substituting (6-16), (6-19), (6-42), (6-43) into (6-41) and rearranging results in

$$I_1 = \frac{1.25C_{L2}f_s}{K}(A_v V_{in} + \frac{7V_{GSat1}}{\beta_2}) \tag{6-44}$$

The power of the current mirror opamp is

$$P = (2I_1 + 2I_2)V_{DD} = 2I_1(1+K)V_{DD} \tag{6-45}$$

Substituting (6-44) into (6-45) results in

$$P = \frac{2.5C_{L2}f_s(1+K)V_{DD}}{K}(A_v V_{in} + \frac{7V_{GSat1}}{\beta_2}) \tag{6-46}$$

Express all the capacitors in terms of unit capacitance and capacitance ratio, (6-46) becomes

$$P = \frac{2.5[n+\beta_2(2+a)]Cf_s(1+K)V_{DD}}{K}(A_v V_{in} + \frac{7V_{GSat1}}{\beta_2}) \tag{6-47}$$

Normally a certain noise level has to be satisfied according to system specification, substituting (6-37) into (6-47), the capacitance term is eliminated and the opamp power can be rewritten as:

$$P = \frac{kTf_b 10(2+a)(1+K)V_{DD}}{v_{tot,in}^2 K}[n(2+a+i)+i(2+a)(1+\frac{2}{3}+\frac{2}{3}n_t)][A_v V_{in} + \frac{7V_{GSat1}(2+a+i)}{i}] \tag{6-48}$$

It is seen from (6-48) that the power is directly inverse proportional to the noise, proportional to the signal bandwidth, and highly dependent on actual circuit implementation. However, the relationship between power and clock frequency is not explicitly shown from the equation. To interpret further, the power of the 1st-order lowpass filter and minimum unit capacitance C vs. sample frequency is plotted in Fig. 6.6 at maximum signal bandwidth of 1.28MHz.

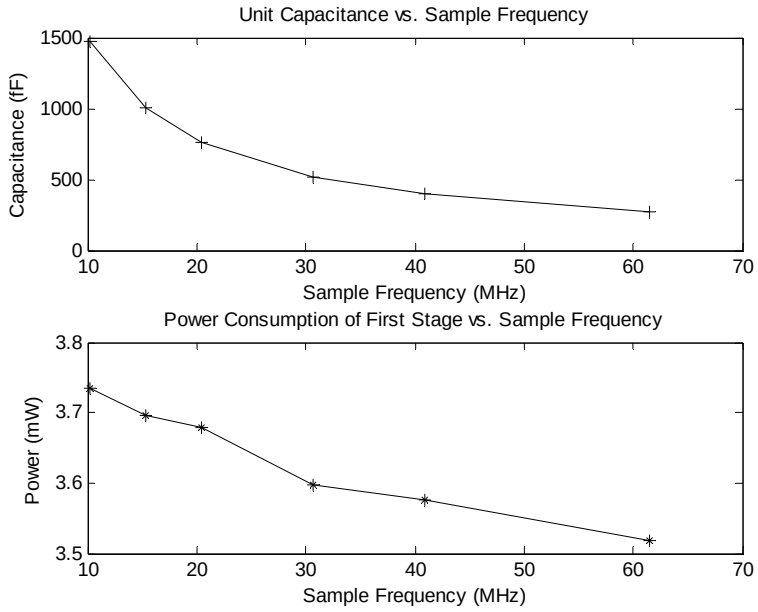


Fig. 6.6 Minimum unit capacitance (upper) and power consumption (lower) vs. sample frequency of the 1st-order lowpass filter at f_b=1.28MHz

In this calculation, the capacitance ratio is varied when sample frequency changes, in order to maintain the same gain and bandwidth for a fair comparison. As show in the figure, the power is a weak function of the sample frequency. High sampling frequency seems a bit superior but the parasitic effects that are neglected in the foregoing calculation will play an increasingly important role and diminish the weak advantage. The result is expectable: for a target noise level, large f_s thus large OSR reduces the in-band noise according to (6-37), so that small unit capacitance can be used to relieve the opamp loading and facilitate low power. However, high frequency requires fast settling, which means a fast hence power hungry opamp. Although doesn't affect the CSF power too much, large OSR can relax the order and attenuation of the preceding anti-aliasing filter, as well as reduce the unit capacitance thus chip area. The above analysis justifies the adoption of equal sampling frequency

of CSF and ADC in this work.

Fig. 6.7 shows the calculated power consumption of the 3rd-order CSF (assuming same opamps are used in all stages) vs. input signal bandwidth f_b at OSR of 16 while keep the same input referred noise power of 5.0588e-9V^2 (equivalent to NF of 37dB at 50Ω). All the other parameters used here are the same as those in the real circuit implementation. As predicted in (6-48), a linear relationship is observed. The measured power is also plotted in Fig. 6.7, showing a good agreement with the theoretical prediction.

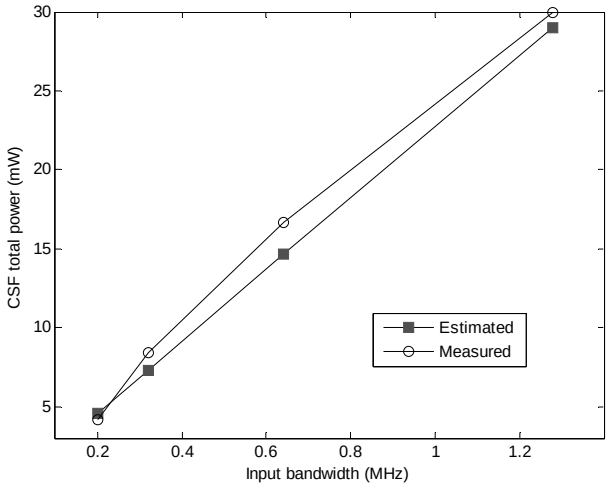


Fig. 6.7 Estimated and measured power of the CSF vs. input signal bandwidth

The power consumption of the 1st-order lowpass filter in the CSF is analyzed in this section. Calculation reveals that to reduce the circuit noise, either oversampling ratio or sampling capacitor has to be increased, both of which requires more power dissipation. In general, the power consumption is larger for a wider signal bandwidth, lower noise level and is highly dependent on the filter and opamp topology.

6.4 Power Dissipation of the ΣΔ A/D Converter

6.4.1 Input-referred Thermal Noise of the SC Integrator

It is well known that, the quantization noise, which is inherent to the quantization procedure, is attenuated in ΣΔ modulators through the combined use of over-sampling and noise shaping. However, even though it is usually accepted that ΣΔ conversion is intrinsically less sensitive to building blocks non-idealities than other data conversion technique, there still exists various error mechanisms for electrical implementations. Fig. 6.8 shows typical noise sources in the ΣΔ modulator. The in-band noise is generally dominated by thermal noise, thus in the following analysis, only thermal noise and quantization noise will be considered.

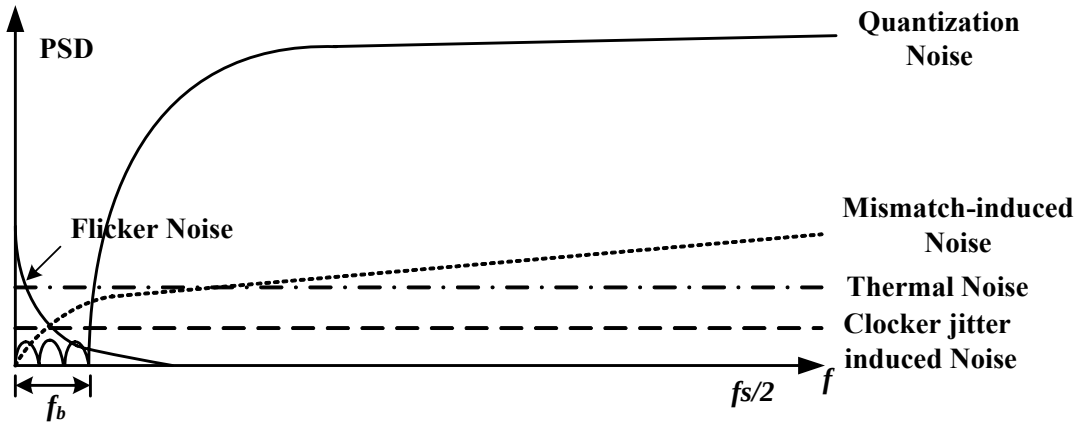


Fig. 6.8 Noise sources in a ΣΔ modulator

The basic building blocks in the A/D converter are the integrators. Moreover, the first integrator in the chain has the greatest influence on the modulator's performance. Since its non-idealities are added directly to the input signal, therefore appears with no filtering in the output spectrum. The contributions to the in-band thermal noise power of the rest of the integrators are attenuated by different powers of the oversampling ratio, depending on the position of the integrator and, in general can be neglected [1].

The power consumed in a SC integrator is generally proportional to its loading.

Consequently to minimize the power dissipation, the smallest capacitor size for which the required converter resolution and bandwidth can be maintained should be used. This noise oriented approach leads to a modulator design, in which the performance is limited primarily by the thermal noise in the first integrator as illustrated in Fig. 6.8.

We begin the analysis by investigating the thermal noise of the integrator. Again, the effects of finite opamp gain and parasitic capacitance are ignored for simplicity. Fig. 6.9 shows the schematic of the 1st integrator in the ΣΔ modulator. Its transfer function is

$$H(z) = \frac{C_s}{C_i} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{6-49}$$

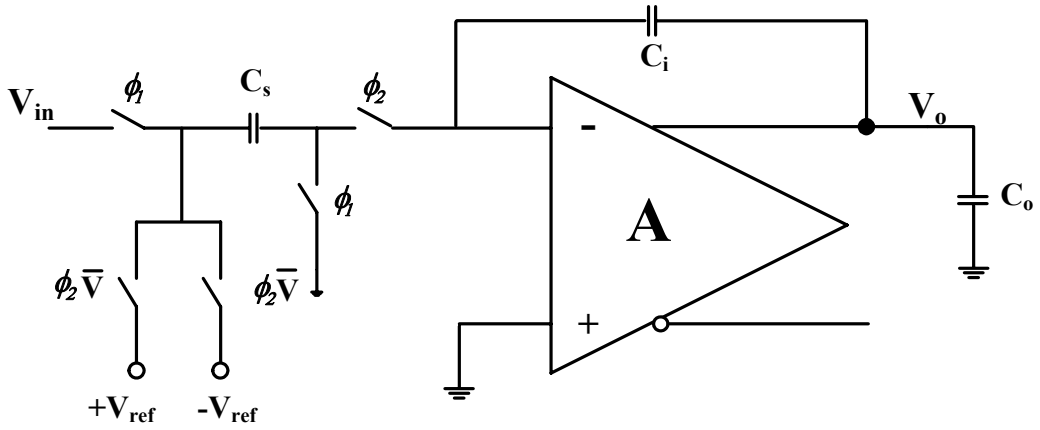


Fig. 6.9 Schematic of the 1st SC integrator

The speed of the circuit is limited by the bandwidth in both clock phases. The -3dB bandwidth is determined by the unity gain frequency of the opamp and the feedback factor. Similar to previous calculation of CSF, denote the feedback factor on ϕ_1 is β_1 while on ϕ_2 is β_2

$$\beta_1 = 1 \tag{6-50}$$

$$\beta_2 = \frac{C_i}{C_s + C_i} \tag{6-51}$$

For a single-stage opamp, the unity-gain frequency is

$$\omega_u = \frac{g_m}{C_{load}} \tag{6-52}$$

The load capacitance on ϕ_1 is C_{L1}, while on ϕ_2 is C_{L2}

$$C_{L1} = C_i + C_o \tag{6-53}$$

$$C_{L2} = C_o + \beta_2 C_s \tag{6-54}$$

where C_o is assumed to be a fixed loading capacitor on both clock phases. Thus the -3dB bandwidth on ϕ_1 is given by

$$\omega_{-3dB,\phi_1} = \beta_1 \omega_{u1} = \frac{g_m}{C_i + C_o} \tag{6-55}$$

while on ϕ_2 is

$$\omega_{-3dB,\phi_2} = \beta_2 \omega_{u2} = \frac{g_m C_i}{C_o(C_s + C_i) + C_i C_s} \tag{6-56}$$

Noise charge from the switches stored on ϕ_1, will transfer to output on ϕ_2 to generate a noise voltage

$$v_{n,\phi 1}^2 = \frac{2kTC_s}{C_i^2} \tag{6-57}$$

Note that a factor of two is included to take into account differential structure and noise from two branches. (6-57) divided by the integrator gain C_s/C_i, the input referred noise on ϕ_1 due to switch is thus

$$v_{ndif,\phi 1}^2 = \frac{2kT}{C_s} \tag{6-58}$$

The noise source on ϕ_2 is from sampling capacitor C_s and opamp noise, which is

usually dominated by the latter as discussed in section 6.3.1. The z-domain output noise from the opamp noise source ($v_{n,amp}$) is again derived based on charge conversion. Neglect the influence of finite bandwidth of the opamp on charge transfer. On clock phase ϕ_1 (t=(n-1)T) we have the total charge

$$q_1 = v_o(n-1)C_i - v_{n,amp1}(n-1)C_i \tag{6-59}$$

where $v_o(n-1)$ denotes the output voltage at time t=(n-1)T, $v_{n,amp1}$ is the noise power due to opamp in ϕ_1. In the next clock phase ϕ_2 (t=(n-1/2)T), the total charge is

$$q_2 = v_o(n-\frac{1}{2})C_i - v_{n,amp2}(n-\frac{1}{2})(C_i + C_s) \tag{6-60}$$

where $v_{n,amp2}$ is the noise power due to opamp in ϕ_2. The total charge in the two clock phases is conserved. Therefore $q_1=q_2$, we have

$$v_o(n-1) - v_{n,amp1}(n-1) = v_o(n-\frac{1}{2}) - v_{n,amp2}(n-\frac{1}{2})\frac{C_i + C_s}{C_i} \tag{6-61}$$

In the next clock phase ϕ_1, the output is held by C_i. So an additional constraint is the charge conservation on C_i, i.e.

$$v_o(n-\frac{1}{2})C_i - v_{n,amp2}(n-\frac{1}{2})C_i = v_o(n)C_i - v_{n,amp1}(n)C_i \tag{6-62}$$

We can now get an expression for the output signal at t=nT from (6-61) and (6-62)

$$v_o(Z^{-1}-1) = v_{n,amp1}(Z^{-1}-1) - v_{n,amp2}Z^{-1/2}\frac{C_s}{C_i} \tag{6-63}$$

Simplify (6-63), we have

$$v_o = v_{n,amp1} + v_{n,amp2}\frac{Z^{-1/2}}{1-Z^{-1}}\frac{C_s}{C_i} \tag{6-64}$$

The output noise is referred to the input by dividing the transfer function of the integrator (6-49), i.e.

$$v_{in} = v_{n,amp1} \cdot \frac{C_i}{C_s} \frac{1 - Z^{-1}}{Z^{-1}} + v_{n,amp2} \cdot Z^{1/2} \tag{6-65}$$

In the case of an over-sampling ΣΔ modulator, the second term will dominate since the first term has a high pass characteristic. $v_{n,amp2}$ can be calculated by

$$v_{n,amp2}^2 = s(f) \cdot BW_n = 2 \cdot \frac{8}{3} \frac{kT(1+n_t)}{g_m} \cdot \frac{\omega_{-3dB,\phi_2}}{4} = \frac{4}{3} \frac{kT(1+n_t)C_i}{C_o(C_s + C_i) + C_i C_s} \tag{6-66}$$

The total input referred noise is the sum of the noises in two clock phases, adding (6-58) and (6-66), we have

$$v_{inn}^2 = \frac{2kT}{C_s} + \frac{4}{3} \frac{kT(1+n_t)C_i}{C_o(C_s + C_i) + C_i C_s} \tag{6-67}$$

The total in-band input referred noise power is thus

$$v_{tot,in}^2 = \frac{4kTf_b}{f_s}\left[\frac{1}{C_s} + \frac{2}{3} \frac{(1+n_t)C_i}{C_o(C_s + C_i) + C_i C_s}\right] = \frac{2kT}{M}\left[\frac{1}{C_s} + \frac{2}{3} \frac{(1+n_t)C_i}{C_o(C_s + C_i) + C_i C_s}\right] \tag{6-68}$$

Again, the noise is reduced for large oversampling ratio *M* and large capacitor.

6.4.2 Power Dissipation of the ΣΔ A/D Converter

The target of this section is to predict the theoretical power consumption of the SC integrator as a function of modulator specification, for example, dynamic range, input signal bandwidth, etc. First, a general expression of ΣΔ A/D converter's power vs. dynamic range is derived.

As can be seen from (6-68), the input referred noise can be expressed in the form of

$$v_{tot,in}^2 = \frac{4kTf_b}{f_s C} \gamma = \frac{2kT}{MC} \gamma \tag{6-69}$$

where γ is a constant determined by capacitance ratio and modulator transfer function.

If the maximum amplitude of the differential input to the modulator is $V_{in,sw}$, then the power of a full-scale sinusoidal input is

$$S_{sig} = \frac{v_{in,sw}^2}{2} \tag{6-70}$$

The dynamic range of the modulator is defined as the ratio of the power in a full scale input to the power of a sinusoidal input for which the signal-to-noise ratio is one. Thus, for a modulator whose in-band noise is dominated by the thermal noise in the first integrator, the dynamic range is

$$DR = \frac{S_{sig}}{v_{tot,in}^2} = \frac{v_{in,sw}^2 MC}{4kT\gamma} \tag{6-71}$$

From (6-71), it follows that

$$C = \frac{(DR)4kT\gamma}{v_{in,sw}^2 M} \tag{6-72}$$

The power consumption in the integrator is

$$P = I_{amp} V_{DD} \tag{6-73}$$

where I_{amp} is the average opamp current and V_{DD} is the supply voltage. In a class A opamp the quiescent amplifier current must be large enough to ensure the load can be charged up quickly enough to accommodate the largest voltage step within a certain integration period. Therefore,

$$I_{amp} = \frac{C\Delta V_{out}}{T_s / 2} \tag{6-74}$$

where ΔV_{out} is the largest differential step change in the output voltage. Assume the integration has to finish with half a clock period ($T_s/2$). ΔV_{out} is given as [3]

$$\Delta V_{out} = \frac{C_s}{C_i}(V_{in,sw} + V_{ref}) \tag{6-75}$$

where V_{ref} is the amplitude of the differential feedback voltage of the modulator as illustrated in Fig. 6.9. Substituting (6-72), (6-74) and (6-75), (6-73) can be rewritten as

$$P = 16kT\gamma f_b(DR)\frac{V_{DD}(V_{in,sw}+V_{ref})}{v_{in,sw}^2} \tag{6-76}$$

If further assume $V_{in,sw}$=V_{ref}=V_{DD}, (6-76) becomes

$$P = 32kT\gamma f_b(DR) \tag{6-77}$$

It is apparent from this general expression that the power is proportional to input signal bandwidth, and dynamic range. On the other hand, the power dissipation is highly dependent on the specific circuit implementation of the ΣΔ modulator, such as, choice of modulator architecture, opamp topology. The following analysis is devoted to the proposed A/D converter for the RFID reader, the specification and circuit implementation of which is discussed in section 5.2.3.

The response of an operational amplifier that employs a differential pair as its input stage typically includes a slew limited region followed by a linear response. Since the integration phase is normally the bottleneck in terms of settling, all the calculation below will assume in the clock phase ϕ_2. The duration of slew limited region is

$$T_{Slew} = \frac{V_f}{S} \tag{6-78}$$

Where V_f is the asymptotic value of the output voltage, S is the slew rate of the amplifier. The maximum value of V_f is

$$V_{f,\max} = \frac{C_s}{C_i}(V_{in,sw}+V_{ref}) \tag{6-79}$$

If the linear settling is characterized by a single pole response, the time duration is

$$T_{Lin} = a\tau \tag{6-80}$$

Where τ is the settling time constant, given by $1/\omega_{-3dB,\phi 2}$, and a is a factor that ensures settling to within 0.5LSB of the modulator [3]. To achieve dynamic range of DR, a can be expressed as

$$a = \ln\sqrt{2DR} = \frac{1}{2}(\ln 2 + \ln DR) \tag{6-81}$$

The sampling time, which is the sum of the slew limited region and linear settling region, should be within half clock period, i.e.

$$\frac{T_s}{2} = \frac{C_s}{C_i S}(V_{in,sw} + V_{ref}) + \frac{1}{2\omega_{-3dB,\phi_2}}(\ln 2 + \ln DR) \tag{6-82}$$

For a single stage opamp, the slew rate is

$$S = \frac{2I_1}{C_{L2}} \tag{6-83}$$

Substituting (6-78), (6-79), (6-80), (6-81) and (6-83) into (6-82) and rearranging results in

$$I_1 = f_s \frac{C_o(C_s + C_i) + C_s C_i}{C_i}\left[\frac{C_s(V_{in,sw} + V_{ref})}{C_s + C_i} + \frac{(V_{GS} - V_{th})}{2}(\ln 2 + \ln DR)\right] \tag{6-84}$$

where I_1 is the drain current of the input transistor.

The total power consumption is highly dependent on the opamp topology and actual implementation. Take the folded-cascode amplifier shown in Fig. 6.10 as an example, the quiescent power dissipated is

$$P = 2(I_1 + I_2)V_{DD} \tag{6-85}$$

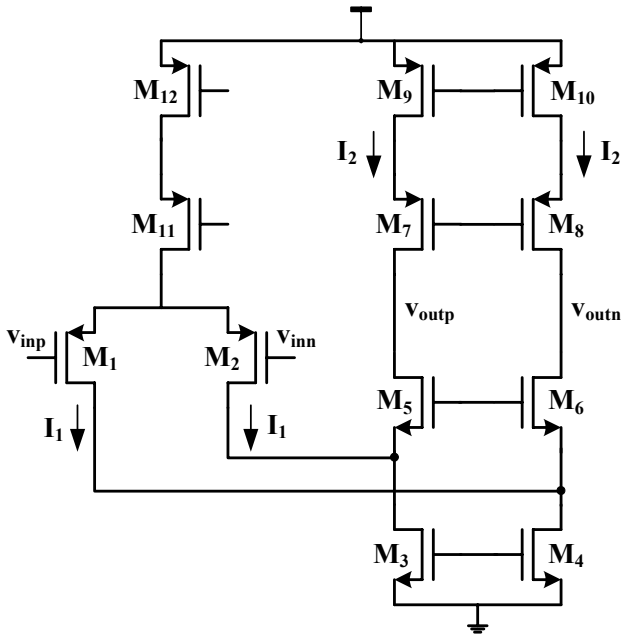


Fig. 6.10 Folded-cascode opamp

In order to equalize the positive and negative slew rate in the two halves of the differential circuit, the M_3 and M_4 must be able to sink a current that is equal to or greater than $2I_1$. Thus

$$I_2 \geq I_1 \tag{6-86}$$

Assume I_2=I_1 for simplicity, the power consumption of the SC integrator can be calculated

$$P = 4 f_s V_{DD} \frac{C_o(C_s + C_i) + C_s C_i}{C_i} [\frac{C_s(V_{in,sw} + V_{ref})}{C_s + C_i} + \frac{(V_{GS} - V_{th})}{2} (\ln 2 + \ln DR)] \tag{6-87}$$

The maximum input signal power for the RFID ADC is about 0.5 V^2 (-3 dBV). If the target dynamic range is α dB, the input referred noise power of the first integrator is $-(3+\alpha)$ dBV, i.e. $10^{-(3+\alpha)/10}$ V^2.

Define C_s=C, C_i=m×C and C_o= n×C , (6-68) can be rearranged to result in:

$$10^{\frac{-3-\alpha}{10}} = \frac{4kTf_b}{f_s C}[1 + \frac{2}{3} \cdot \frac{(1+n_t)m}{n(1+m)+m}] = \frac{2kT}{MC}[1 + \frac{2}{3} \cdot \frac{(1+n_t)m}{n(1+m)+m}] \tag{6-88}$$

Substituting (6-88) into (6-87), the power consumption is obtained

$$P = \frac{16kTf_bV_{DD}}{10^{\frac{-3-\alpha}{10}}}[\frac{n}{m}+n+1+\frac{2}{3}(1+n_t)][\frac{(V_{in,sw}+V_{ref})}{m+1}+\frac{(V_{GS}-V_{th})}{2}(\ln 2+0.23\alpha)] \quad (6\text{-}89)$$

As a conclusion, in general, the power of the ΣΔ A/D converter is proportional to its DR and signal bandwidth as seen in (6-77). For a specific circuit, once the order and transfer function are determined, 1) for a given DR α, which means the OSR M is fixed (see (6-90)), the power is proportional to input bandwidth f_b; 2) for a given input bandwidth f_b and target DR α, the power is insensitive to the OSR M according to (6-89), to the 1st-order estimation. Although large OSR requires fast opamp, it leads to smaller capacitor, thus relaxed opamp driving requirement, which compensates the power increase to a certain extent.

6.4.3 Reconfigurability of the ΣΔ A/D Converter

One major advantage of the ΣΔ A/D converters is that they can trade resolution in amplitude with oversampling ratio in time, i.e. their inherent reconfigurability. This section elaborates the effects of oversampling ratio and input signal bandwidth on the ADC's dynamic range and power consumption, seeking a systematic way to optimize the ADC's power for different performance requirement.

If only quantization noise is taken into account, the dynamic range of an L[th]-order, multibit ΣΔ modulator is given as [6]

$$DR = 10\log[\frac{3}{2}(2^B-1)^2\frac{(2L+1)}{\pi^{2L}}M^{2L+1}] \quad (6\text{-}90)$$

where L is the modulator order, B is quantizer's resolution. Hence, it is apparent that for a high order modulator, the quantization noise will rise quickly when M is reduced, because of the M^{2L+1} relationship.

The A/D converter in this work is first designed for the largest dynamic range. At OSR of 24 a 4th-order MASH 2-1-1 modulator is chosen, and corresponding loop coefficients are designed. Some of the other design parameters are listed below: C_s = 0.75pF; C_i= 3pF; $V_{in,sw}$=1V_{pp}; V_{ref} =1.5V_{pp}. The maximum input signal power for the ADC is 0.5 V^2 (-3 dBV), the quantization noise alone is thus calculated as

$$v_{in,q}^2 = 10^{-0.3}[\frac{3}{2}(2^B-1)^2\frac{(2L+1)}{\pi^{2L}}M^{2L+1}]^{-1} \quad (6\text{-}91)$$

while the thermal noise can be calculated by (6-68).

In this work, the ADC sampling capacitor is fixed. At OSR of 24, the quantization noise level is 1.32e-10 V^2, while the input referred thermal noise power is 7.33e-10 V^2. In this case, the thermal noise dominates and limits the DR to 88.3dB. When *M* changes to 16, the thermal noise increases to 1e-9 V^2, but the quantization noise increases much quicker, to 5.1e-9 V^2, which is larger than thermal noise and becomes the dominate noise, so the DR is reduced to 80dB. On the other hand if increasing the *M* to 32, the quantization noise power scales down to 1e-11 V^2, while thermal noise is 5.5e-10 V^2, therefore thermal noise limits the DR to about 90dB. Fig. 6.11 shows the calculated power consumption of the 1st integrator and ADC's DR vs. oversampling ratio. For fixed capacitor at OSR of 20 or higher, DR is limited by thermal noise; while for OSR below 20, DR is limited by quantization noise in the proposed A/D converter. It is seen that only changing the OSR to vary DR is not an optimal solution, because when OSR is reduced, it is not power efficient to maintain the same capacitor which is too large for a decreased DR. As also seen in Fig. 6.11, if assume the capacitance can be decreased with *M* and DR without limit (ignore the

layout matching issue) and quantization noise equals the thermal noise, the ideal power consumption shows a logarithmic dependency on *M*. Therefore, the most optimal solution is to adjust the OSR and capacitor simultaneously. Whereas the challenge of this approach is tuning large amount of capacitors while keep the ratio unchanged.

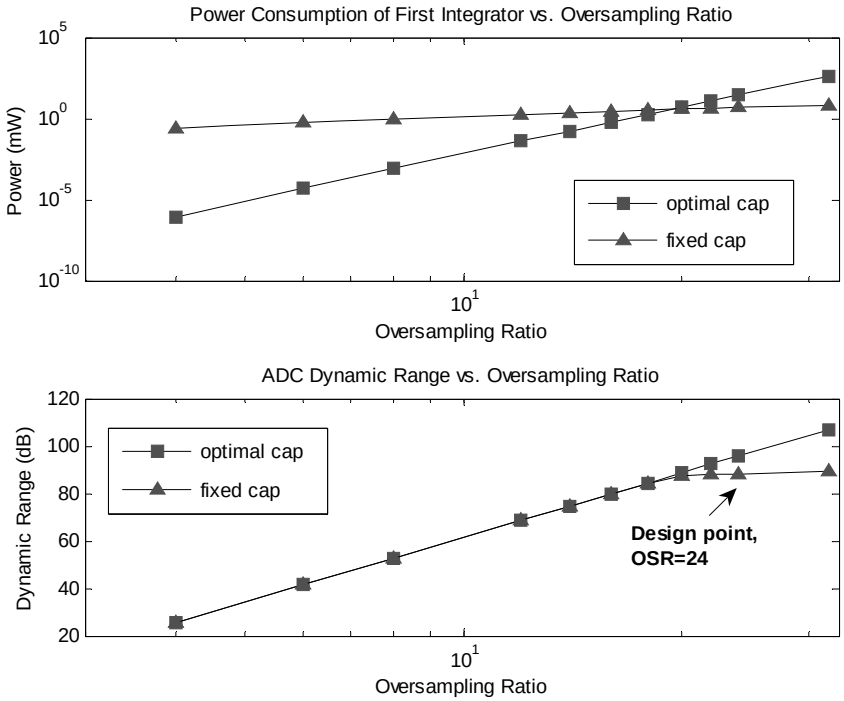


Fig. 6.11 Calculated power consumption of the 1st integrator and ADC's dynamic range vs. OSR

Fig. 6.12 plots the calculated ADC power (assuming same power for all the four opamps) vs. the input bandwidth f_b for OSR=24 and OSR=16 based on ADC's design parameters, in comparison with the measured power. Similar to CSF, and as can be seen in (6-89). ADC's power shows a linear dependency on the input signal bandwidth f_b for a given DR. The characteristic can be utilized to optimize the power for different input signal bandwidth, especially for system like RFID which features

a variable bandwidth.

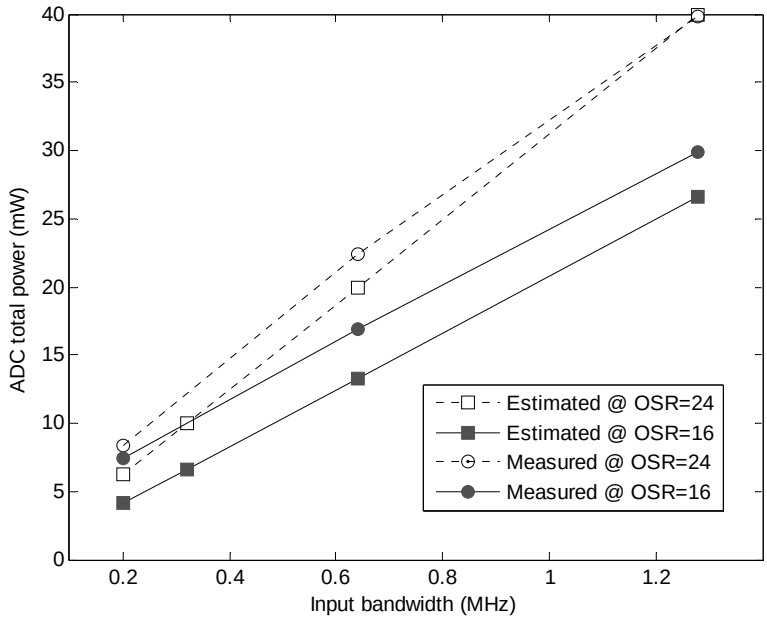


Fig. 6.12 Calculated and measured power consumption of the ADC vs. input signal bandwidth for OSR=16 and OSR=24

6.5 Power Dissipation of the Decimation Filter

For integrated digital circuits like the decimation filter, switching power consumption is currently the most significant part of the total power consumption. It is due to the current drawn from the power supply to charge the parasitic capacitors (also called load capacitance made up of gate capacitance, diffusion capacitance and interconnect/wire capacitance). Switching energy consumption is proportional to the switching activities, as well as the load capacitance and the square of the supply voltage. It is mathematically determined by the following well-known equation

$$P_{dec\_filter} = CV_{DD}{}^2 f_{clk} \tag{6-92}$$

where C is the switching capacitance of the circuit, and f_{clk} is the clock frequency driving the digital filter, which is directly p sroportional to the receiving data rate and

thus input bandwidth of the receiving signal. (6-92) again implies the power consumption of a fixed decimation filter design has a linear relationship with the signal bandwidth. Fig. 6.13 illustrates the simulated decimation power consumption for OSR=16 and OSR=24 vs. clk frequency.

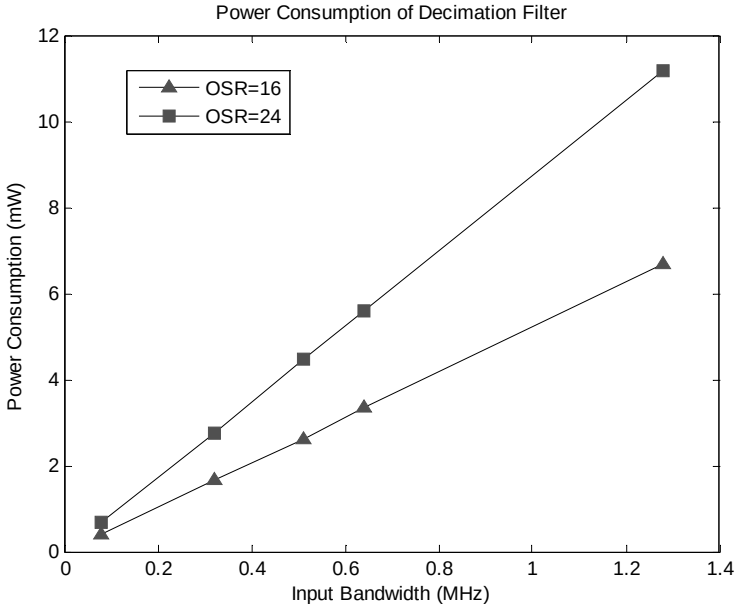


Fig. 6.13 Simulated power consumption of the digital decimation filter

6.6 Power Dissipation of the Baseband vs. Dynamic Range

6.6.1 Relationship of Baseband Filtering and ADC Dynamic Range

The order of the channel selection filter and ADC's dynamic range can be traded with each other as discussed in section 2.3.3. A higher order filter leads to a low resolution ADC while a low order filter must be combined with a high-resolution (dynamic range) ADC to cope with large difference between signal and blockers [7]. Assume the sensitivity of the receiver is P_{sen}, the largest blocker is P_{blo}, the difference between the two power levels is the receiver's ability to reject interference, we define it the dynamic range of the receiver, given by $\delta=P_{blo}-P_{sen}$. Suppose the attenuation of

blockers by filter is ρ dB. The ADC should not be the dominant noise source for a power efficient implementation [8]. If we set the ADC's noise level to be 20 dB lower than the RX sensitivity. The dynamic range specification of ADC can be calculated by

$$DR_{ADC} = P_{blo} - \rho - P_{sen} + 20 = \delta - \rho + 20 \tag{6-93}$$

We will further assume in the filter, one order can provide 6dB/oct attenuation. Define the order of the filter to be N_f, then the total achievable attenuation at adjacent channel is $6N_f$ dB. In the RFID system, the largest blocker is the adjacent channel interference with the magnitude of -35dBm. For a target receiver sensitivity of -90dBm

$$DR_{ADC} = \delta - 6N_f + 20 = 75 - 6N_f \tag{6-94}$$

Approximately a 3rd-order filter leads to a 10-bit ADC. If no filtering present, the ADC dynamic range can be as high as 75dB, i.e., more than 12 bits.

6.6.2 A Systematic Approach for Power Optimization

The target of this section is to find a systematic way to optimize baseband power consumption subject to the constraints on the noise, system dynamic range δ and settling time, i.e. signal bandwidth. We will combine the power estimation results obtained for the filter and A/D converter respectively and their relationship discussed in 6.6.1, trying to seek an optimal solution.

As discussed, to achieve a system dynamic range of δ dB, we can either choose a higher order filter or a large dynamic range A/D converter. Suppose the power of each opamp is the same in the CSF, i.e., we didn't aggressively perform power

scaling in the filter. This is the actual scenario in the proposed CSF, in which gain is mainly allocated in the first stage of the filter so that the later stages' noise becomes unimportant. High gain stage means high power opamp as shown in foregoing analysis in chapter 4 and section 6.3.1, because large gain means a small feedback factor, which reduces the closed-loop bandwidth and settling time. In the biquad, on the other hand, smallest possible capacitors can be used, which essentially are limited by layout and matching, to relieve the opamp loading. But most of the attenuation is achieved in the biquad so that it needs to settle fast enough to accomplish accurate transfer function, which necessitates an opamp with large unity-gain frequency and slew rate. Therefore, the power of the 3rd-order CSF is simply N_f times the power of a single stage, according to (6-48)

$$P_{CSF}=\frac{10kTf_b(2+a)(1+K)V_{DD}N_f}{v_{tot,in}^2K}[n(2+a+i)+i(2+a)(1+\frac{2}{3}+\frac{2}{3}n_t)][A_vV_{in}+\frac{7V_{GSat1}(2+a+i)}{i}]$$

(6-95)

For the L^{th}-order A/D converter, again assume the opamp power is the same in each integrator for simplicity. Since the dynamic range of the A/D converter is given by (6-94), substitute it into (6-89) and multiply L, the total power of the A/D converter is

$$P=\frac{16kTf_bV_{DD}L}{10^{\frac{-\delta+6N_f-23}{10}}}[\frac{n}{m}+n+1+\frac{2}{3}(1+n_t)][\frac{(V_{in,sw}+V_{ref})}{m+1}+\frac{(V_{GS}-V_{th})}{2}(5.29+0.23\delta-1.38N_f)]$$

(6-96)

Fig. 6.14 and Fig. 6.15 shows the calculated power of the baseband vs. CSF order N_f at f_b=1.28MHz for a target δ of 55dB and several ADC's OSR M. The procedures are as follows:

1) For a given δ and N_f, calculate the ADC's DR, and increase several dB to account for DR degradation due to other noise sources in the ADC that are not considered in the foregoing discussion.

2) For each OSR M, assume thermal noise dominates for a power efficient ADC implementation, and calculate the value of sampling capacitor. Furthermore, limit the minimum acceptable capacitance to 50fF due to layout and mismatch consideration, i.e. if the resultant capacitor is smaller than 50fF, adopt 50fF.

3) Since in step 2), only thermal noise is tackled. Compare the quantization noise and thermal noise, make sure quantization noise is at least 3dB below the thermal noise by increasing order L. In such a manner, the minimum order L for each OSR M is obtained based on (6-91).

4) Total power consumption of the baseband is then calculated, which only includes the CSF and ADC. The decimation filter power is not counted, because its implementation hence its power dissipation would be highly dependent on the ADC order L and M (see section 5.4.1). Moreover, as depicted in Fig. 6.13, the power of the decimation filter is less than that of analog circuits (about 1/6 of the analog power) therefore can be neglected during the initial optimization.

As shown in Fig. 6.14, the power of ADC increases fast when the attenuation of CSF is small, because in a thermal noise dominated design, every 3dB increase in ADC's DR leads to double of its power consumption. It can also be seen that a reasonably large OSR reduces the ADC order, thus ADC power. However, as the sampling frequency increases further, neglecting the parasitics and other higher order effects

causes an increased inaccuracy in the estimation. In this work, the design point where ADC is 24 times oversampled and CSF exhibits a 4^{th}-order characteristic is close to the optimal solution as shown in Fig. 6.15.

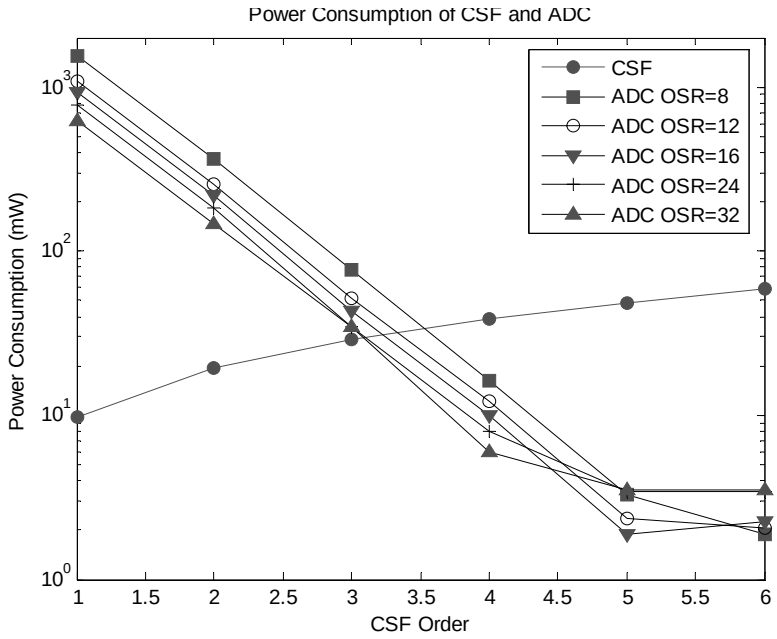


Fig. 6.14 Power consumption of CSF and ADC respectively vs. CSF order for different ADC OSR (f_b=1.28MHz and δ of 55dB)

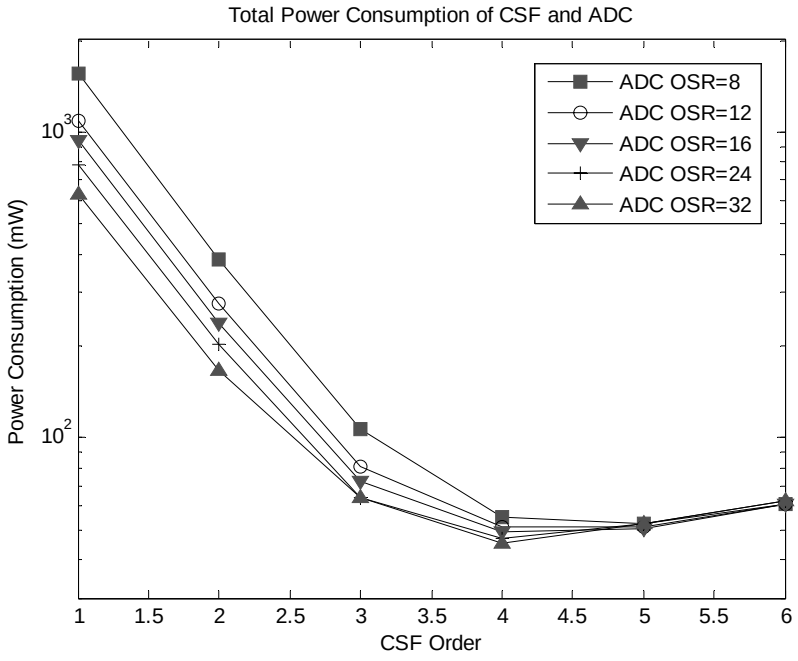


Fig. 6.15 Total power consumption of analog baseband vs. CSF order for different

ADC OSR (f_b=1.28MHz and δ of 55dB)

The calculated minimum order L and corresponding minimum sampling capacitor is illustrated in Fig. 6.16. As expected, when OSR is increased, for the same amount of channel selection filtering, sampling capacitance and ADC order can be reduced.

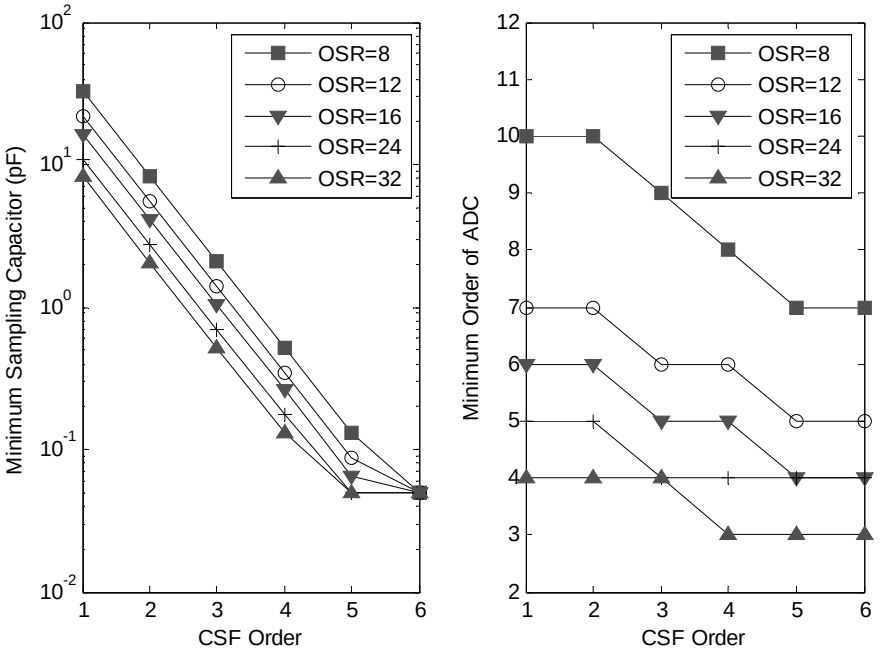


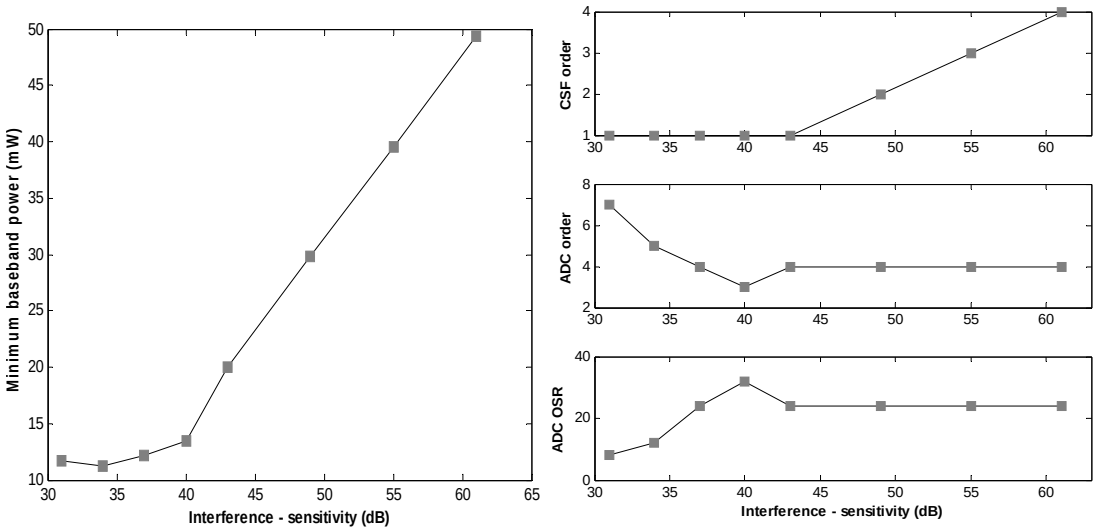
Fig. 6.16 Min capacitance and min order of ADC vs. CSF order for different ADC OSR (f_b=1.28MHz and δ of 55dB)

To investigate the influence of system dynamic range on the optimal distribution of filtering and ADC DR, calculations are performed with δ altered and all the other parameters kept the same. As shown in Fig. 6.17 (b), when δ is small, the digital channel selection tends to outperform (CSF order is reduced). Since ADC power doubles for every 3dB increase in the dynamic range, for application with low system dynamic range, its power reduces significantly.

As a conclusion, a systematic way for baseband power optimization is discussed in this section. Following this approach, for a given system dynamic range and

bandwidth, optimal allocation of filtering and ADC design parameter can be found which minimizes the total power consumption. To cope with different electromagnetic environment for multi-protocol operation, mixed-mode channel selection approach is the most power efficient to handle large interference while bypassing the analog filter and using digital channel selection is favorable for relaxed interference scenario. As such, the baseband operation is reconfigured into 3 modes in this work: ADC and CSF both sampled at OSR=16; ADC sampled at OSR=24 with CSF bypassed; ADC sampled at OSR=16 with CSF bypassed.

It is worth mentioning that this analysis is only the first order estimation, in which various parasitic effects are not included, such as the comparator power consumption, parasitics capacitors in the opamps, phase noise of the interferer, etc. As a result, enough design margins are required to allow the degradations in the real circuit implementation. In the measurement, we find that to achieve 55dB dynamic range at 1.28MHz, filter attenuation has to be 25dB larger than the estimated value and the total baseband power is almost doubled. Nevertheless, the trend predicted by the theory provides good design guidance.

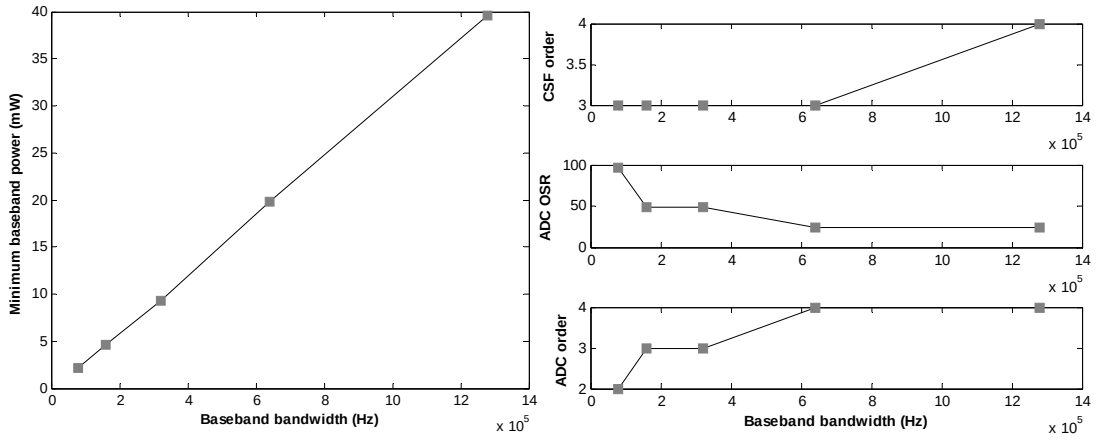


(a) (b)

Fig. 6.17 (a) Min baseband power consumption vs. δ; (b) corresponding CSF and ADC parameters at min baseband power (f_b=1.28MHz)

6.7 Power Dissipation of the Baseband vs. Bandwidth

To further investigate the influence of bandwidth on the optimal baseband architecture, the same design parameters and procedure in previous section are utilized in the calculation for different signal bandwidth from 80 kHz to 1.28MHz. As illustrated in Fig. 6.18, for the target system dynamic range δ of 55dB, mixed-signal channel selection approach again shows advantage (CSF order is 3 or 4). Although at optimal point the configurations of CSF and ADC are different for different bandwidths, an almost linear relationship between power and bandwidth is still observed. For the RFID system, in which the tag-to-reader data rate, thus receiver baseband bandwidth is varied, the proposed mixed-signal baseband architecture is a favorable solution in that power can be adjusted dynamically for different data rate.



(a) (b)

Fig. 6.18 (a) Min baseband power consumption vs. f_b; (b) corresponding CSF and

ADC parameters at min baseband power (δ=55dB)

In practical implementation, we may not be able to adapt the CSF and ADC design parameters once the designs are fixed, resulting in sub-optimal solutions. However, even for fixed design of CSF, ADC and decimation filter, we have proved the power consumption of all stages has a linear dependency on the input signal bandwidth for the same noise and dynamic range in section 6.3.2, 6.4.2 and 6.5. Thus the total power is expected to be linearly increasing with speed. Fig. 6.19 plots the calculated power consumption of the three baseband stages vs. input bandwidth for one baseband configuration, i.e. CSF and ADC both on and sampled at OSR=16. Fig. 6.20 illustrates the calculated baseband total power vs. input bandwidth for three different configurations. Fig. 6.19 and Fig. 6.20 are based on fixed design parameters of CSF and ADC in this work.

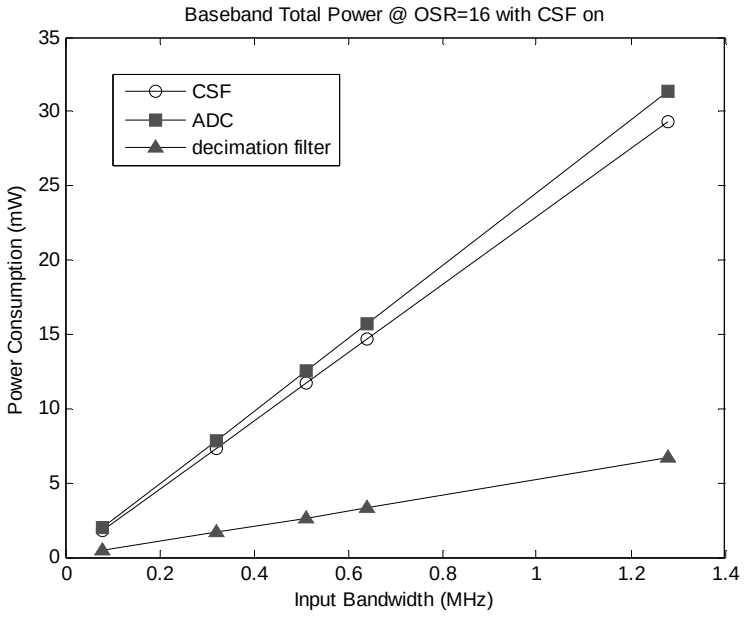


Fig. 6.19 Power consumption of the three baseband stages vs. input bandwidth (OSR =16 and with CSF on)

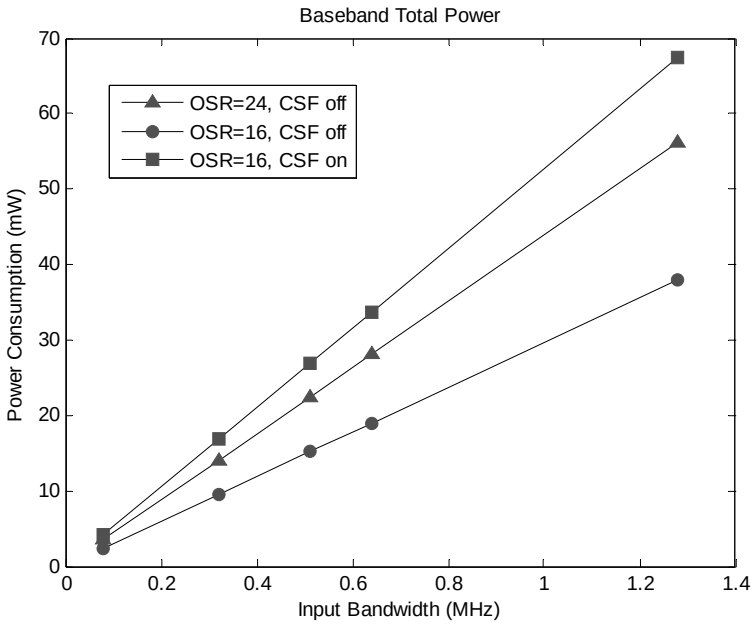


Fig. 6.20 Baseband total power vs. input bandwidth for three configurations

6.8 Summary

The reconfigurable baseband is studied in depth in this chapter. In architecture level, theoretical analysis reveals that an optimal distribution between filtering and ADC dynamic range exists for a given speed and noise which minimizes the total baseband power. In particular, for relaxed dynamic range, the analog filter should be bypassed and digital channel selection outperforms, but for medium to high dynamic range, mixed-signal channel selection proves to be more power efficient. In circuit level, like pure digital circuit, the proposed baseband shows a linear power dependency on signal bandwidth, therefore analog bias current can be reduced accordingly at low signal bandwidth.

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Chapter 7
EXPERIMENTAL RESULTS OF THE RFID READER

7.1 Floorplan and Die Micrograph of the RFID Reader

Fig. 7.1 shows the layout floorplan of the reader. For such complicated mixed-signal system floorplan, there are a few criteria: first, for best matching and shortest signal path, especially at high frequency, the building blocks are mainly located following the signal flow; second, it is crucial to minimize the distance hence loading between LO1, LO2 and up-mixer, down-mixer, because in the reader talk mode operation, the RX and TX are on simultaneously; third, for mixed-signal system, special attention is paid to isolate the digital part and the analog part; finally, necessary internal pad are properly placed for performance characterization of the individual building blocks.

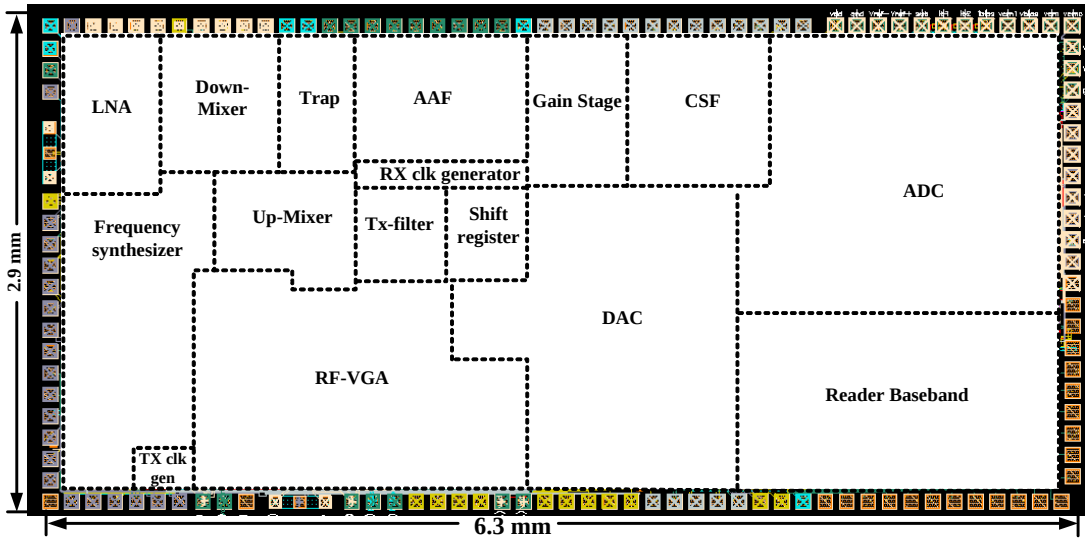


Fig. 7.1 Layout floorplan of the proposed RFID reader

The proposed RFID reader transceiver is fabricated in a 0.18μm CMOS process with 6 metal layers. It occupies a chip area of 2.9mm×6.3mm. The die micrograph is illustrated in Fig. 7.2.

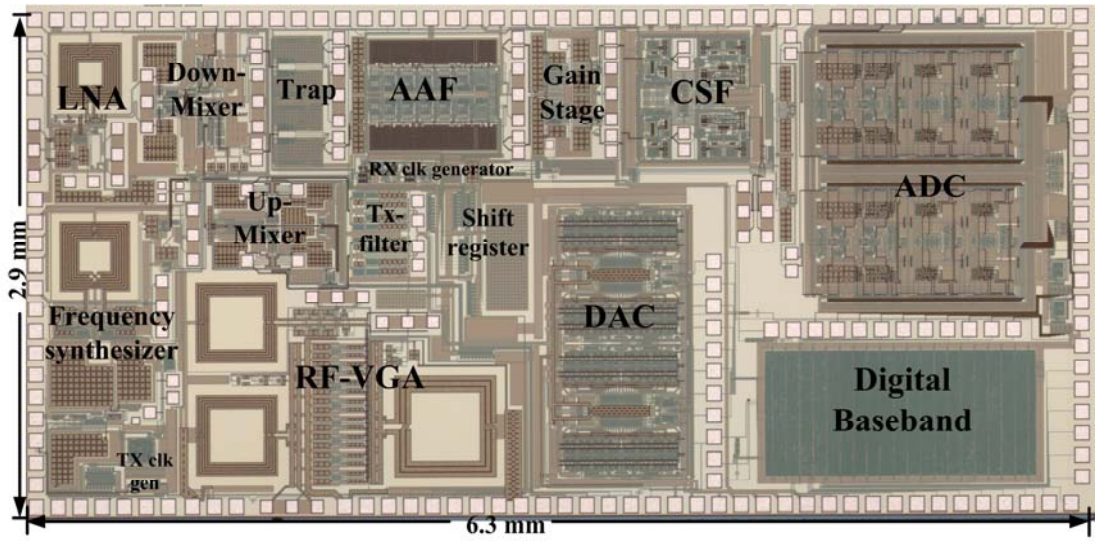


Fig. 7.2 Die micrograph of the proposed RFID reader

7.2 Measurement Setup

After the performance of each building block is fully characterized, the system measurements are carried out. Fig. 7.3 illustrates the basic setup for RX measurement. Input is applied by SGS probe to LNA while the buffered outputs at each stage are obtained by on-wafer probing one at a time. Power combiners/splitters (H-183-4 for LNA, ZFCSJ-2-2-S for baseband) and bias-Ts (ZFBT-4R2GW) are inserted for differential (on-chip signal) to single-end (equipment) conversion. HP80000 pattern generator is utilized to generate clocks to switched-capacitor filters, ADC and DAC. In RX gain measurement, a single tone input is generated by Agilent E4438C signal generator. Agilent E4440A Spectrum analyzer is used to measure the output frequency domain spectrum. Agilent 8753E network analyzer is utilized to measure the frequency response and the IQ mismatch of the RX. In RX noise and SNR

measurement, since the baseband bandwidth is <10MHz, the noise figure meter cannot be used. Output noise floor is measured by Agilent E4440A Spectrum analyzer, hence output SNR can be obtained. In RX IIP3 measurement, two tones of equal amplitudes generated by the Agilent E4438C with its option 408 “enhanced multi-tone signal studio” are input to the LNA. The tone spacing is always equal to the channel bandwidth since our RX features a tunable bandwidth. Output and IM3 of each stage is observed by the Agilent E4440A Spectrum analyzer. For the test of interference rejection and effect of the CW, two signal generators HP8657B and Agilent E4438C are utilized. For RX with ADC, the ADC output is stored in HP16702A logic analyzer and processed by matlab on PC.

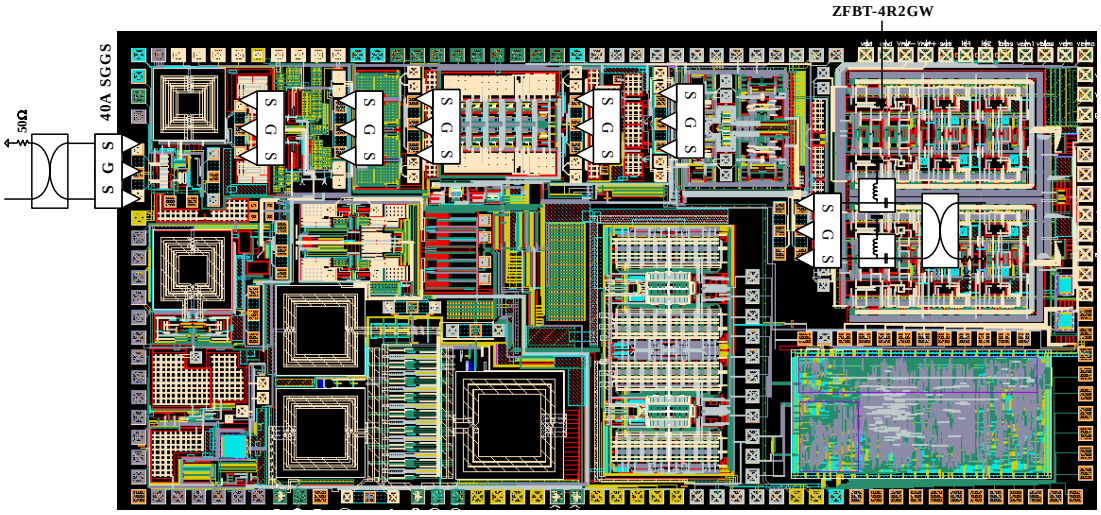


Fig. 7.3 RX measurement setup

Fig. 7.4 illustrates the basic setup for TX measurement. The transmitting baseband IQ signal to the TX filter is generated by the Agilent E4438C vector signal generator. The output of the RF-VGA or external PA (EMPOWER 1075-BBM3Q6A3E) is observed using Agilent E4440A Spectrum analyzer. When testing TX with DAC, the pattern generator HP16702A is utilized to input the baseband data to DAC. Again,

power splitter/combiner with different feature bandwidths are required to provide differential to single-end conversion while bias-Ts are used to generate proper DC bias voltage.

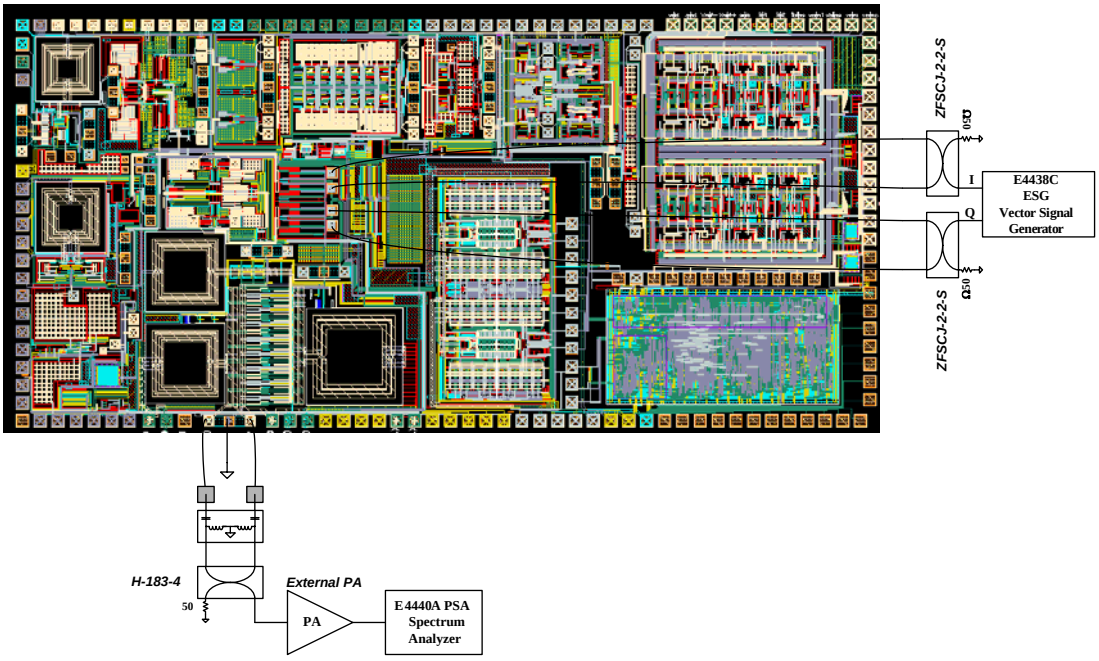


Fig. 7.4 TX measurement setup

7.3 Measurement Results of the Receiver

7.3.1 Receiver Linearity, Bandwidth and Gain

The linearity of the RX front-end is the most critical to deal with the large self-interferer. As shown in Fig. 7.5, for the listen mode operation with LNA turned on, the RX front-end measures P-1dB of –9.4dBm and IIP3 of 0dBm. In the talk mode with LNA bypassed, the RX front-end measures P-1dB of 3.5dBm, IIP3 of 18dBm.

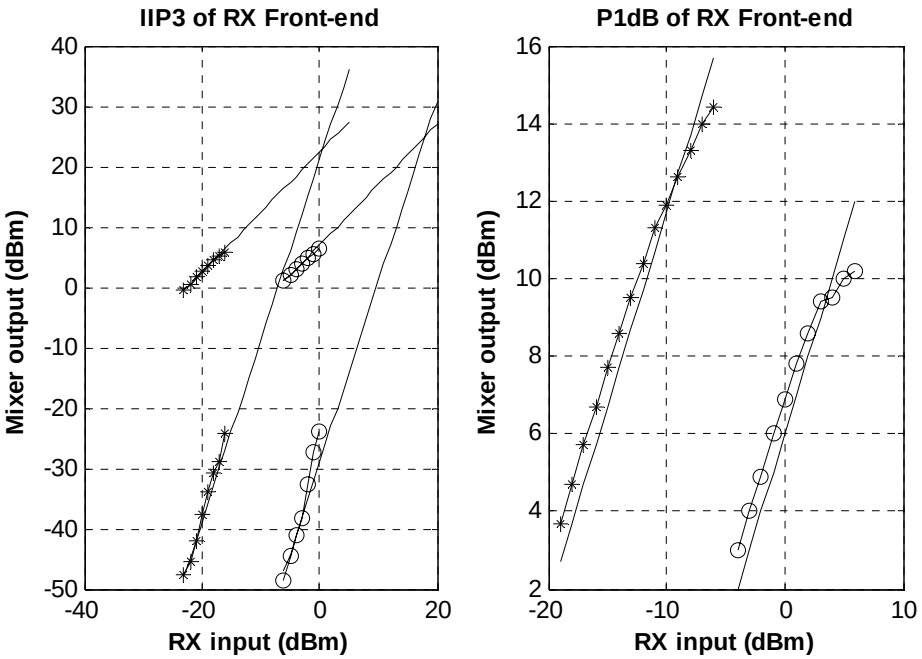


Fig. 7.5 Linearity of the RX front-end

At small gain of 20dB, the RX gain distribution is as follows: LNA -2dB, mixer 8dB, baseband 14dB. The whole RX measures a worst case out-of-band IIP3 of 3dBm at min bandwidth, while the out-of-band IIP3 at max bandwidth is 10dBm as illustrated in Fig. 7.6. The degradation at small bandwidth is mainly due to the reduced amount of filtering of out-of-band interferer when the filters are tuned and the slight linearity degradation in the AAF. As shown in Fig. 7.6, the measured P-1dB of the whole RX is -14.5dBm at min bandwidth and 20dB gain setting.

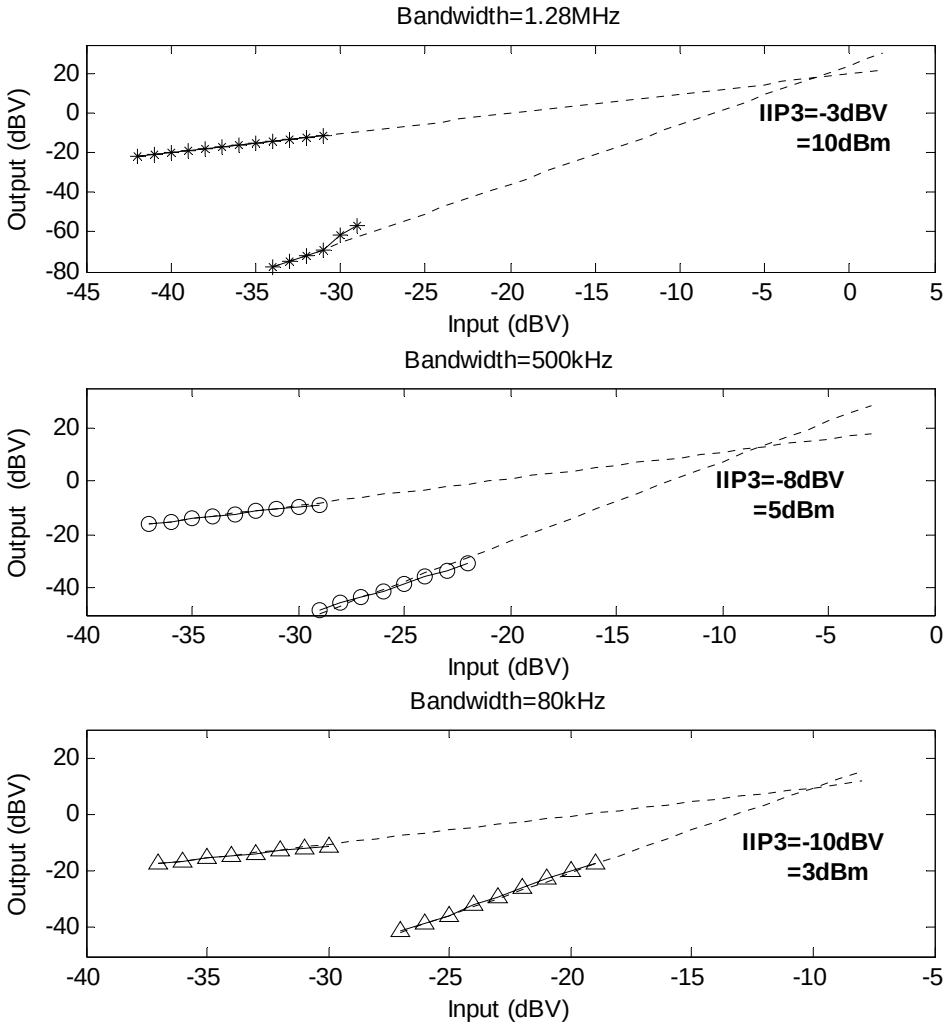


Fig. 7.6 IIP3 of the RX for bandwidth of 1MHz, 500kHz and 120kHz (at 20dB gain with LNA bypassed)

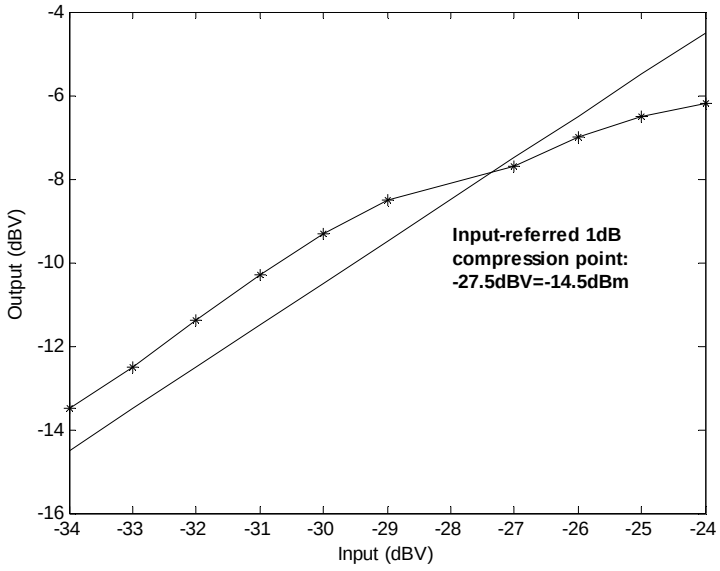


Fig. 7.7 RX P-1dB at minimum bandwidth and 20dB RX gain

The RX gain can be tuned from 10dB to 94dB in 1dB/step resolution. The measured frequency response of the RX is shown in Fig.7.8 with CSF on and maximum gain. The baseband bandwidth is variable from 80 kHz to 1.2MHz, while the adjacent channel rejection is larger than 65dB at largest BW and reduced to 40dB at smallest BW. The maximum gain shows small variation, within 1.5dB, across the whole RF frequency range of 860MHz to 960MHz.

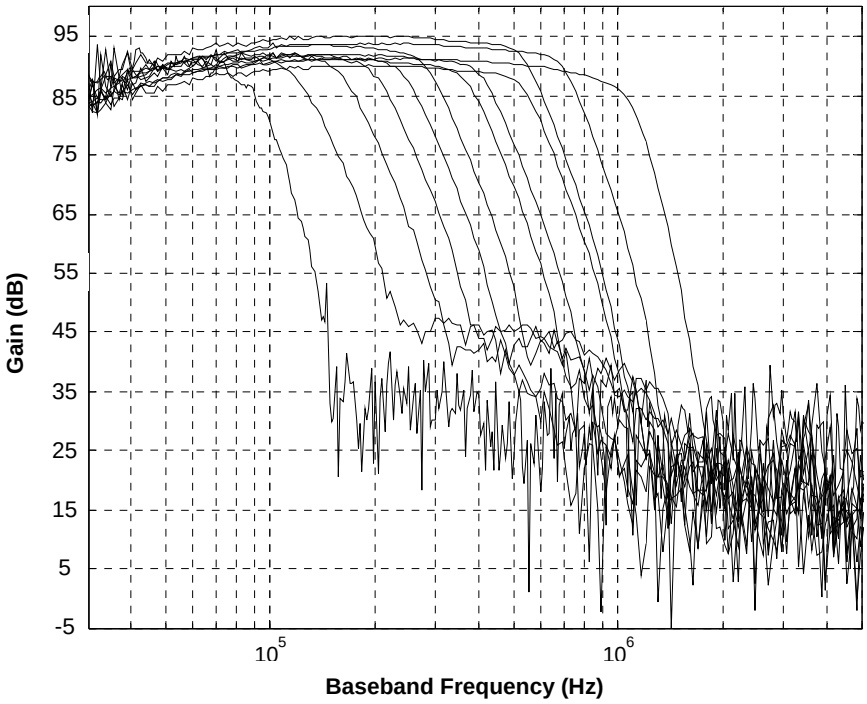
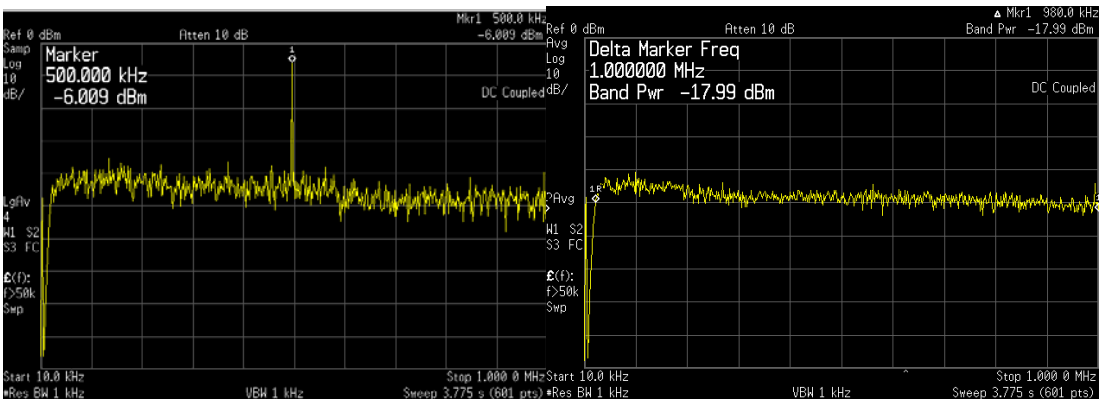


Fig. 7.8 RX frequency response at maximum gain

7.3.2 Receiver Sensitivity, SNR and NF

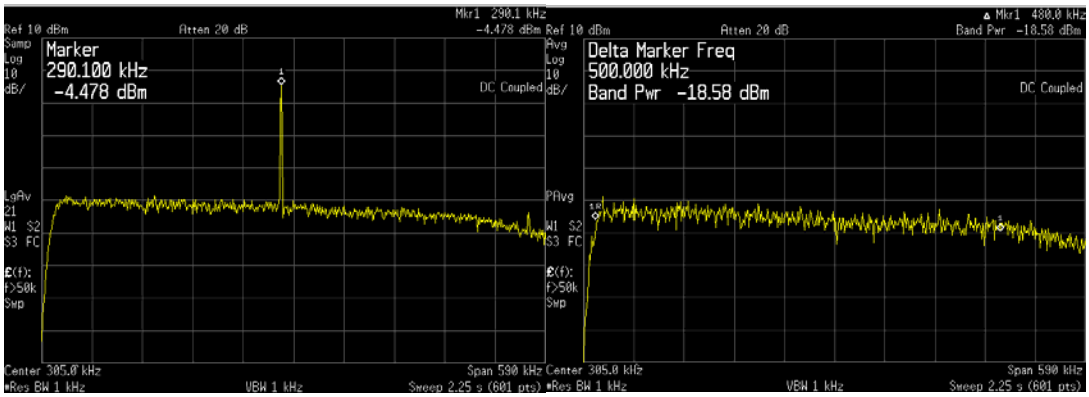
In listen mode, the RX sensitivity is measured to be better than -90dBm. Fig. 7.9 and Fig. 7.10 illustrate the RX CSF output signal and noise floor for an RF input of -90dBm at baseband BW=1MHz and BW=500 kHz respectively. At 1MHz, the output signal to noise ratio is 12dB, which corresponds to a RX NF of *174-90-10log(1M)-12=12dB*. At 500 KHz, the output signal to noise ratio is 14.1dB,

which corresponds to a RX NF of *174-90-10log(500k)-14.1=12.9dB*. The listen mode RX leveling diagram is shown in Fig. 7.11.



(a) (b)

Fig. 7.9 RX SNR_{out} at the CSF output for BW=1MHz (a) signal (b) integrated noise



(a) (b)

Fig. 7.10 RX SNR_{out} at the CSF output for BW=0.5MHz (a) signal (b) integrated noise

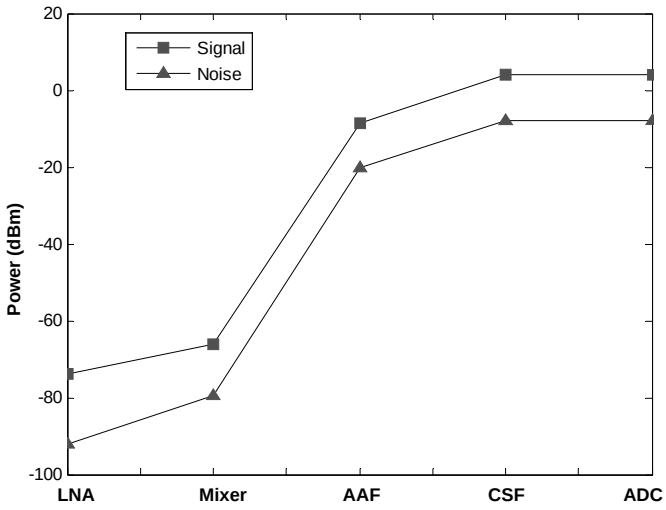


Fig. 7.11 RX leveling diagram

7.3.3 Receiver IQ Mismatch

The RX IQ mismatch is measured with Agilent network analyzer 8753E in frequency offset mode as shown in Fig. 7.12. Without any separate gain tuning, the gain mismatch is 0.6dB while the phase mismatch is 3 deg as illustrated in Fig. 7.13. It corresponds to an image rejection ratio of 27.1dB as depicted in Fig. 7.14. The time domain output waveform is shown in Fig. 7.15, which is measured by HP infinium oscilloscope (500MHz, 1Gsa/s). Summarized in table 7.1, the maximum RX output DC offset voltage is 4mV.

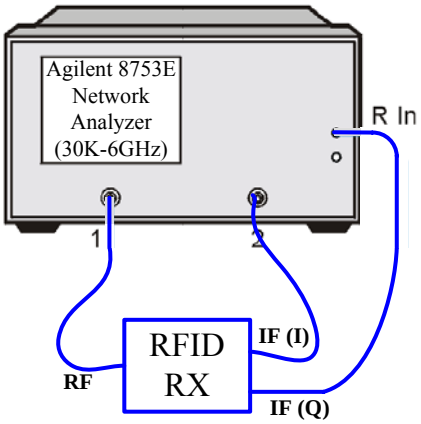


Fig. 7.12 RX IQ mismatch testing setup

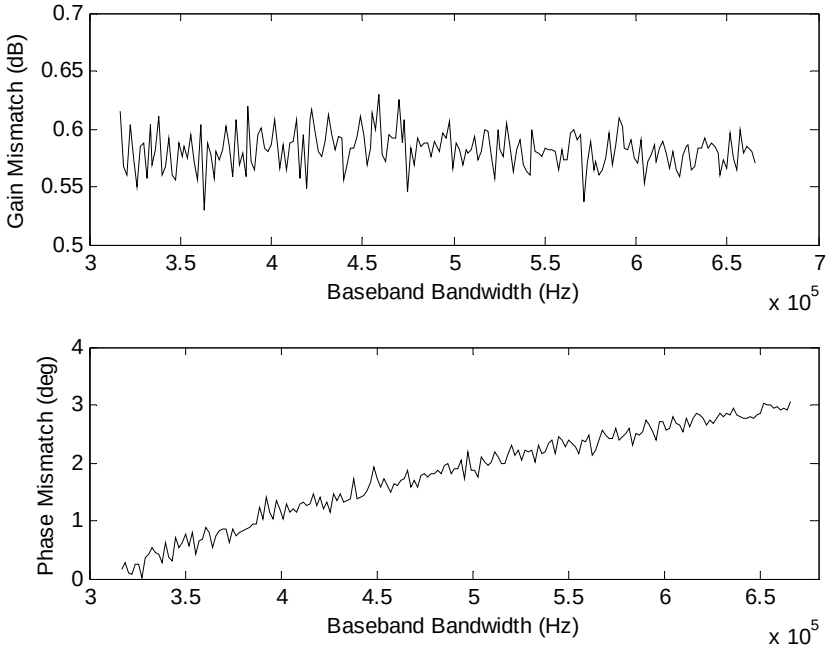


Fig. 7.13 Measured RX I&Q gain and phase mismatch

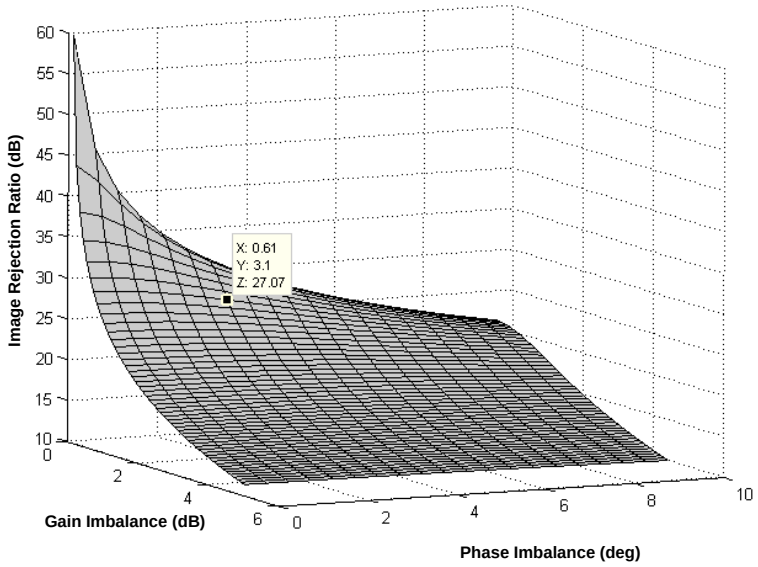


Fig. 7.14 Image rejection ratio vs. gain and phase mismatches

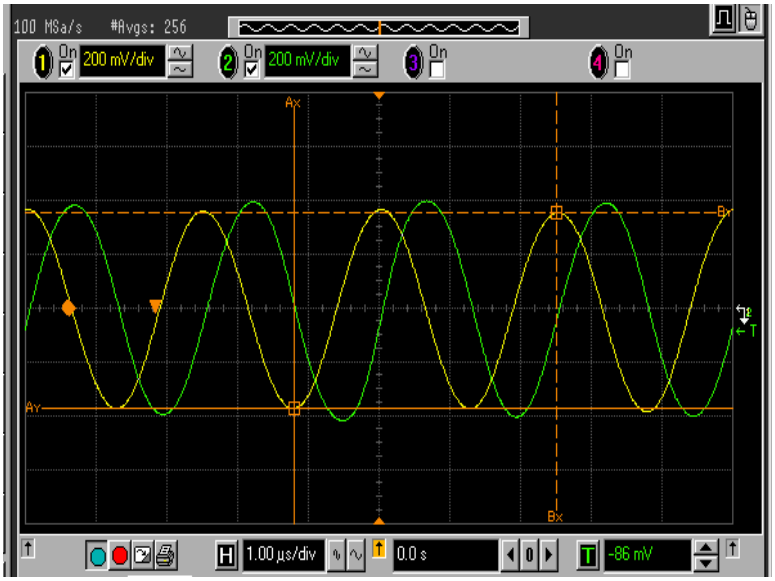


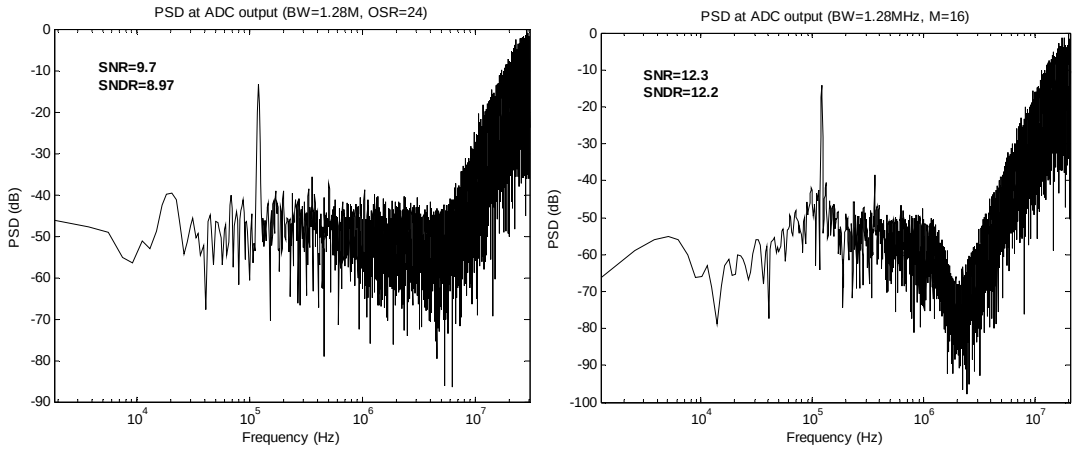
Fig. 7.15 Measured RX IQ outputs at max gain

Table 7.1 Measured DC output voltage of each stage

Stage	Iout+ (V)	Iout- (V)	Qout+ (V)	Qout- (V)
Mixer	0.614	0.589	0.558	0.551
AAF	0.691	0.712	0.678	0.747
Gain stage	1.164	1.167	1.198	1.196
ADC	0.888	0.892	0.91	0.909

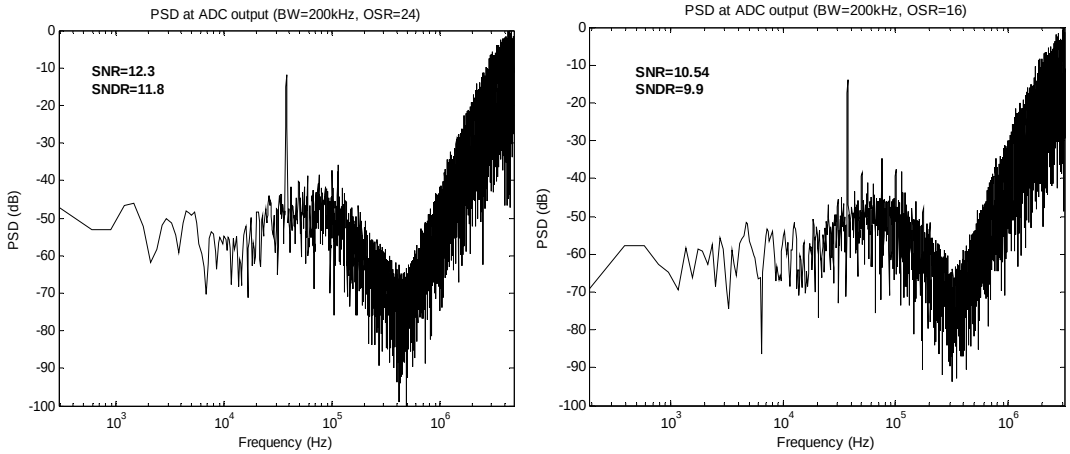
7.3.4 Receiver Interference Rejection Ability with ADC

The RX output SNR is also measured at the ADC output. Fig. 7.16 illustrates the output SNR for an RF input of -90dBm at maximum bandwidth of 1.28MHz and OSR of 24 and 16 respectively. The SNR is degraded at OSR of 24 mainly due to increased distortion of the ADC when the clock frequency is increased to 61.44MHz as can be viewed from raised noise floor at passband edge shown in Fig. 7.16(a). Fig. 7.17 illustrates the output SNR for an RF input of -90dBm at small bandwidth of 200 kHz and OSR of 24 and 16 respectively.



(a) (b)

Fig. 7.16 Measured RX SNR at ADC output for input=-90dBm and BW=1.28MHz (a) OSR=24 (b) OSR=16

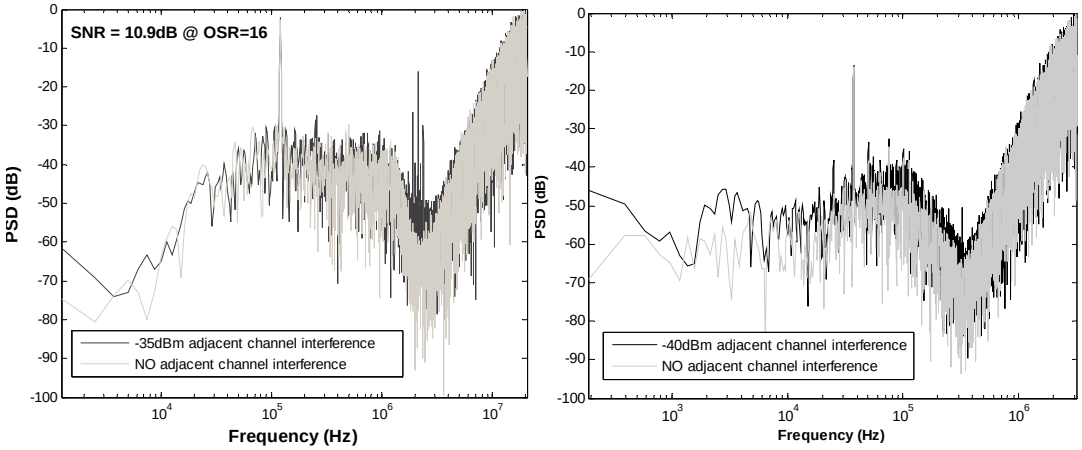


(a) (b)

Fig. 7.17 Measured RX SNR at ADC output for input=-90dBm and BW=200 kHz (a) OSR=24 (b) OSR=16

As discussed in Chapter 6, there are three baseband configurations for different interference rejection requirement. To illustrate the interference rejection ability of the proposed RFID reader, large adjacent channel interferer is applied together with a small desired signal to examine the effect on the RX performance. As an example,

following configuration is chosen: at OSR=16, the CSF is turned on to enhance the attenuation. As depicted in Fig. 7.18 (a), at maximum bandwidth, the SNR_{out} shows negligible degradation for an adjacent channel interferer of -35dBm. However, when the BW is reduced, adjacent channel interference locates closer to the desired signal. As a result, its close-in phase noise significantly raise the in-band noise floor, hence degrades the SNR, as illustrated in Fig. 7.18 (b). To keep the same interference rejection ability, large ADC OSR may be employed to improve the dynamic range for small data rate as shown in Fig. 7.19.



(a) (b)

Fig. 7.18 Measured RX SNR at ADC output for input=-90dBm (a) OSR=16, BW=1.28MHz (b) OSR=16, BW=200 kHz

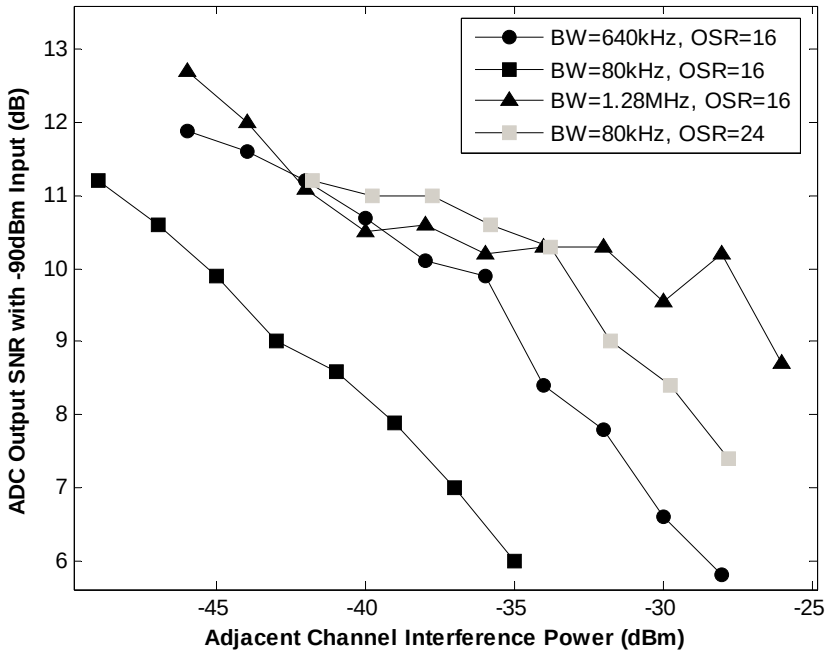


Fig. 7.19 Measured RX interference rejection ability

The interference rejection ability and RX power is measured for three data rates, each with three baseband configuration. As shown in Fig. 7.20, the trend is as expected. However, there are a few discrepancies compared with theoretical study in Chapter 6. First one is the influence of interferer phase noise. In general large interference can be tolerated at large signal bandwidth. While for small bandwidth, the phase noise of the close-in adjacent channel interferer becomes significant noise contributor. Secondly the necessary filter attenuation is considerably larger for the target system dynamic range. They are caused by all the unpredicted mechanisms in the analysis, such as the phase noise of interferer, non-ideal behavior and other noise sources of the ADC, gain compression and nonlinearity of the RX circuits due to the presence of the large interferer, etc. The total RX power shows a substantial tuning range, which proves the effectiveness of the reconfigurable baseband in terms of power optimization.

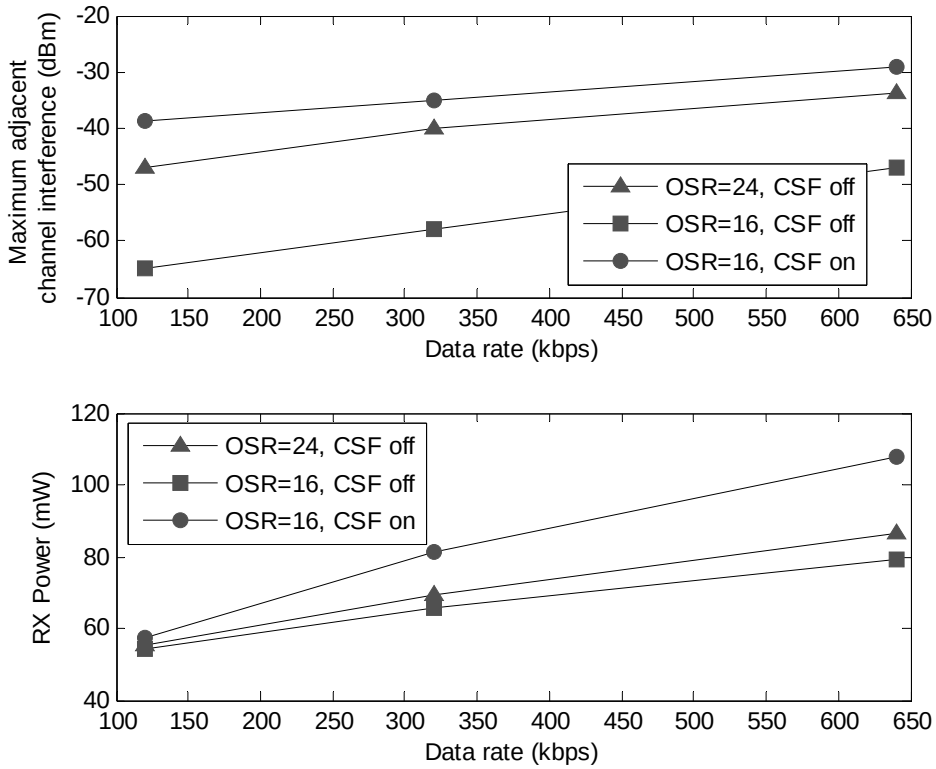
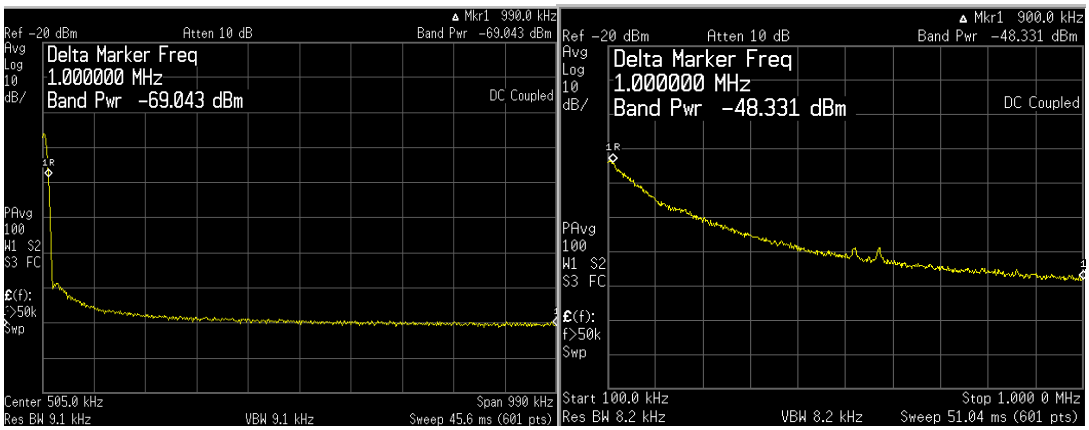


Fig. 7.20 RX power and interference rejection vs. data rate

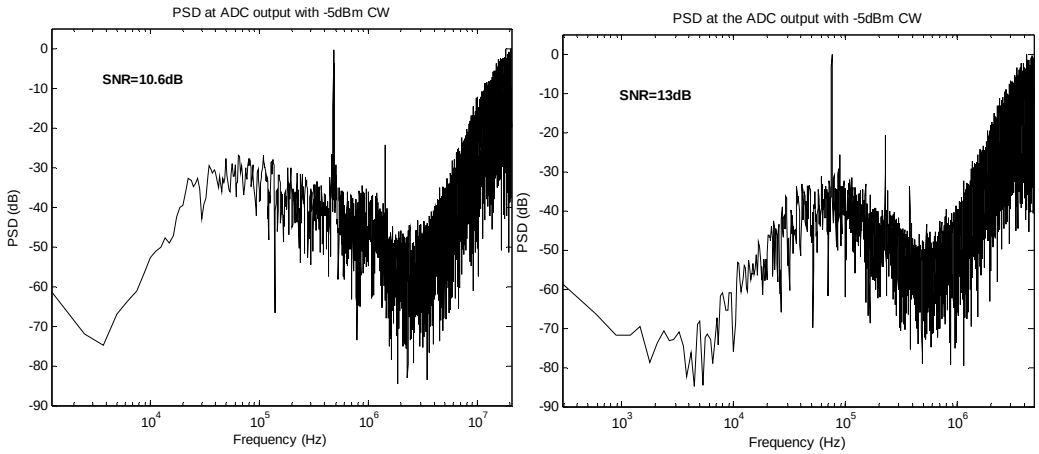
7.3.5 Receiver Sensitivity with Self-interferer

The effect of the self-interferer is investigated theoretically in chapter 2. In order to verify its effect, a single-tone with large amplitude and located at the same frequency as the LO is added together with the small desired signal. As shown in Fig. 7.21, with LNA bypassed, the down-converted phase noise of a -5dBm CW causes a 20dB increase in the AAF output noise floor. It translates to 20dB degradation in the sensitivity, in consequence, the RX sensitivity in talk mode reduces to -70dBm. The measured spectrum at ADC output with a -70dBm desired signal and -5dBm CW is illustrated in Fig. 7.22 for two bandwidths.



(a) (b)

Fig. 7.21 Noise floor at AAF output (a) without CW (b) with CW



(a) (b)

Fig. 7.22 ADC output SNR with CW (a) BW=1.28MHz (b) BW=200kHz

7.4 Measurement Results of the Transmitter

The transmitter achieve output referred 1dB compression point of 10.4dBm without external PA and better than 30dBm with external PA as illustrated in Fig. 7.23. The OIP3 is measured to be 18dBm without external PA and larger than 50dBm with external PA as shown in Fig. 7.24. It is seen that the linearity is dominated by the on-chip RF-VGA rather than the external PA.

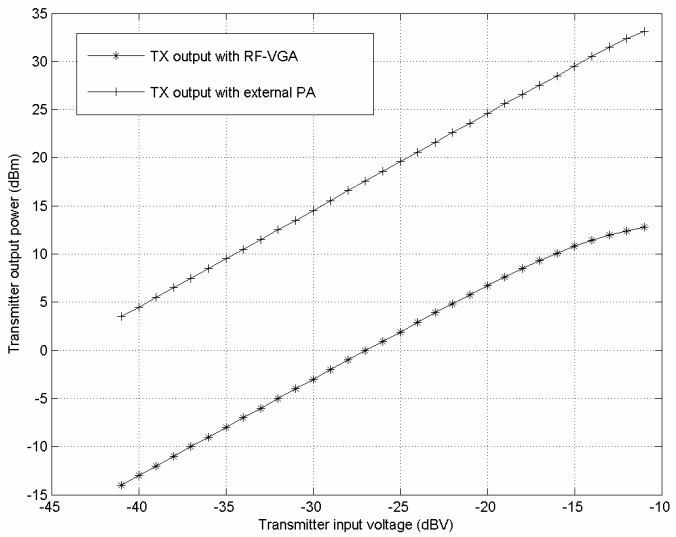


Fig. 7.23 TX output power and output referred 1dB compression point

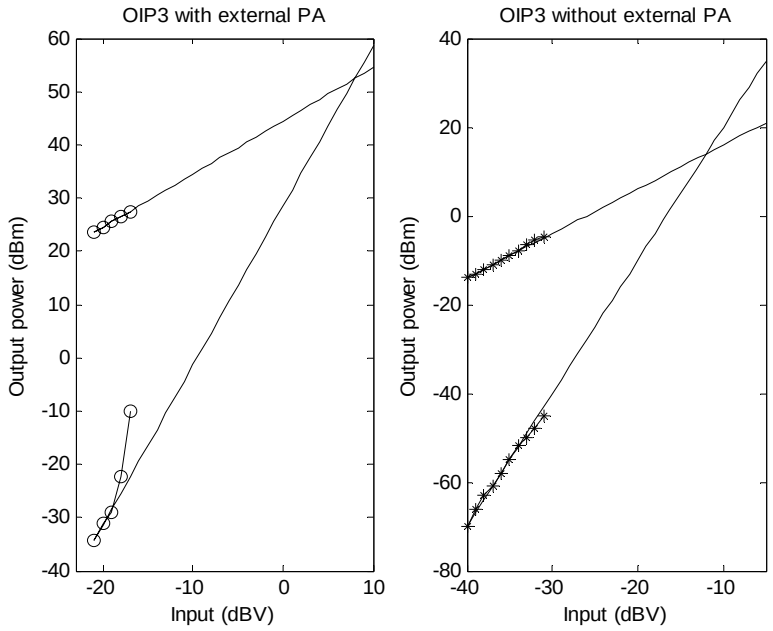


Fig. 7.24 TX OIP3 with and without external PA

The TX measures a sideband rejection of -53dBc as illustrated in Fig. 7.25. The baseband PIE encoded DSB-ASK data is input to the DAC by pattern generator and output spectrum is measured. As can be seen in Fig. 7.26, the TX output closely resembles that of baseband. The output spectrum fulfills the EPC Gen-2 spectrum mask in dense reader mode as shown in Fig. 7.27.

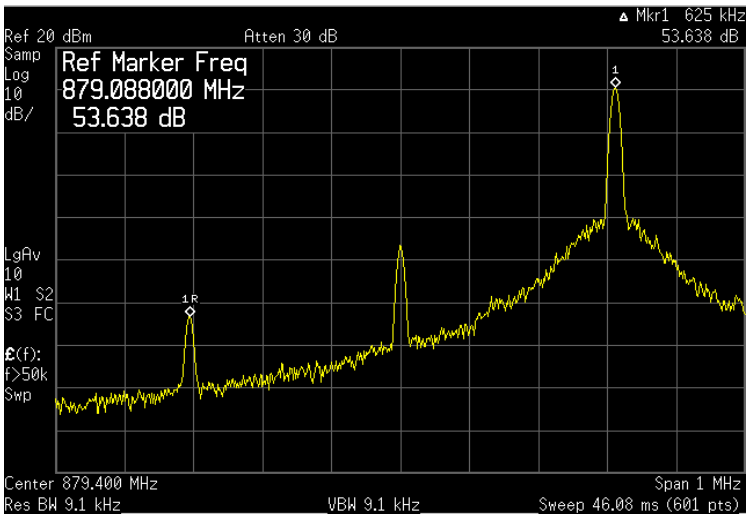


Fig. 7.25 TX sideband rejection ratio

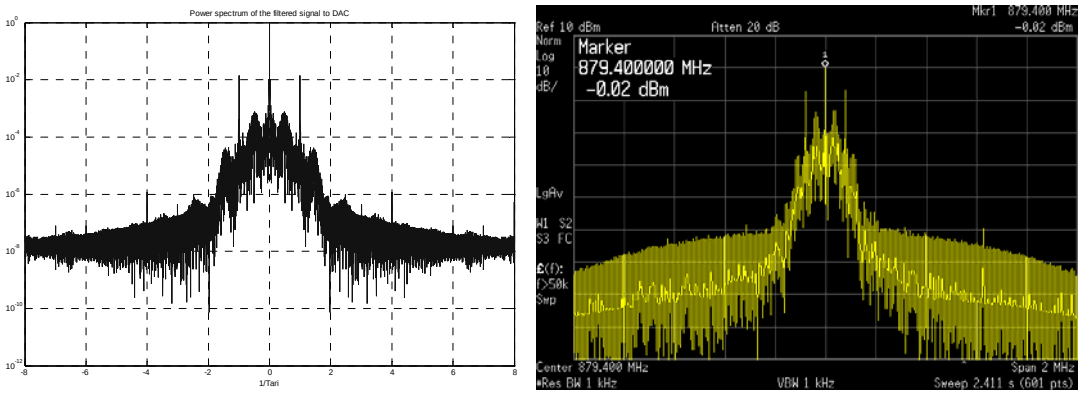


Fig. 7.26 TX output spectrum (a) at baseband output (b) at RF-VGA output

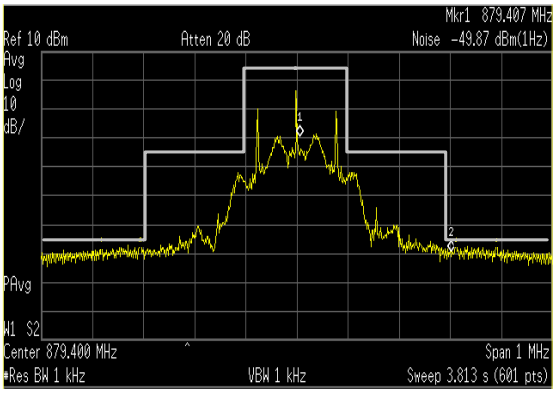


Fig. 7.27 TX output spectrum

7.5 Performance Summary of the Transceiver

The single-chip UHF RFID reader is demonstrated in 0.18μm CMOS technology. The High linearity RX front-end and low phase noise synthesizer are proposed to

handle the large self-interferer. Reconfigurable baseband architecture allows power optimization for the multi-protocol operation. It dissipates a maximum power of 249mW when transmitting maximum output power of 10.4dBm and receiving the tag's response of –70dBm in the presence of –5dBm self-interferer. Table 7.2 summarizes the performance of the proposed RFID reader transceiver. Table 7.3 shows the power breakdown of the transceiver, the RX building blocks are operated at 1.8V because of the stringent linearity requirement. The synthesizer, DAC and PA are operated at 1V supply for best balance between performance and power dissipation, while the up-mixer is still operated at 1.8V for high linearity.

Table 7.2 Performance summary of the proposed RFID reader transceiver

Operating Frequency		860MHz to 960MHz
RX		
Listen mode	Front-end P1-dB	–9.4dBm
	Front-end IIP3	0dBm
	Noise figure (BW=1MHz)	12dB
	RX sensitivity	–90dBm
Talk mode	Front-end P1-dB	3.5dBm
	Front-end IIP3	18dBm
	RX sensitivity (-5dBm self-interferer)	–70dBm
IIP3 (small gain)		>3dBm
P1-dB		>–14.5dBm
Gain range		10dB to 94dB
Channel bandwidth		80KHz to 1.2MHz
Output SNR		11dB
IQ gain mismatch		0.6dB
IQ phase mismatch		3°
Output DC offset voltage		4mV
TX		
Side-band rejection		–53.6dBc
Output P-1dB w/o PA		10.4dBm
Output P-1dB w/ PA		>30dBm
OIP3 w/o PA		18dBm
OIP3 w/ PA		>50dBm

ACPR	30dBc
Frequency Synthesizer	
Phase noise @ 880MHz	–110dBc/Hz @ 200kHz –126dBc/Hz @ 1MHz
Fractional spur	<–70dBc
Reference spur	<–84dBc
Frequency resolution	25kHz
Frequency tuning range	1.06GHz to 1.4GHz
Technology	0.18μm 1P-6M CMOS
Die size	18.3mm^2

Table 7.3 Power breakdown of the proposed RFID reader transceiver

Building blocks		Supply voltage (V)	Power consumption (mW)
RX	LNA	1.8	18.7
	Down-mixer	1.8	21.6
	Active trap (IQ)	1.8	1
	AAF (IQ)	1.8	9
	CSF (IQ)	1.8	30
	ADC (IQ)	1.8	39.8
RX total			120.1
Frequency synthesizer		1	7.4
TX	DAC (IQ)	1	4
	Up-mixer	1.8	28.8
	RF-VGA	1	103.2
TX total			136

7.6 Measurement of the Transceiver with Digital Baseband

After performance characterization of individual parts, the reader TX is measured with digital baseband. The command is input from pattern generator, processed by the digital baseband ASIC. The outputs are then input to the DAC and output spectrum is observed in the PA output for several commands. Fig. 7.28 illustrates the measured PA output. More noise is observed in the output spectrum compared with the one obtained by pattern generator input shown in Fig. 7.26(b), mainly due to

reduced driving capability of the on-chip interface and increased delay. But it still can fulfill the EPC Gen-2 mask in dense reader environment.

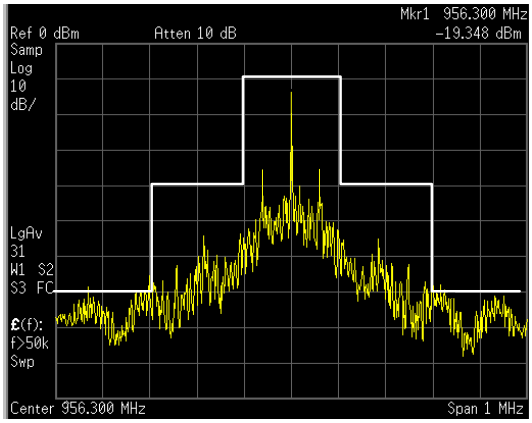


Fig. 7.28 Measured TX output spectrum with digital baseband

The RX measurement with digital baseband ASIC implementation is not carried out mainly due to the following problems. First, the ΣΔ ADC digital cancellation circuit is not able to properly function, which is an important interface between the TRX and digital baseband. Secondly, there is careless mistake in the interface of the decimation filter and RX front-end processor. The decimation filter output scaling coefficient is incorrect so that the baseband fails to generate a proper output. To complete the demonstration of the complete reader, the ADC digital noise cancellation part needs to be modified. Also, the baseband design should be improved including a proper scaling coefficient, and more attenuation hence higher order of the decimation filter to improve the stopband attenuation which is only about 30dB in the current design.

In order to verify the design algorithm, field-programmable gate array (FPGA) prototyping is performed. The Xilinx Virtex-II xc2v1500 platform is used as shown in Fig. 7.29 (a). ModelSim is used for co-verification simulation. Functional tests for

FPGA are done in the same way as that for the chip testing. Agilent Logic Analyzer set which includes a pattern generator embedded is utilized. Input testvectors are generated by using the Simulink model. The output can be monitored through the waveform or listing windows of the logic analyzer. Figure 7.29 (b) shows the setup of the hardware testing. The design is tested and found to be functional as predicted by the RTL model. As predicted by Fig. 5.36, with an SNR of about 11dB, the BER of ASK FM0 is 10^{-3} while much better for other coding and modulation scheme, for example, BER of ASK miller-subcarrier (M=2) can be lowered to 0.6×10^{-3}. On the other hand, the measured receiver output SNR at ADC output is 12dB at OSR of 24 as show in Fig. 7.17, which is more than sufficient to achieve a target BER of 10^{-3} for FM0 ASK and lower than 10^{-3} for the other coding and modulation scheme. For the worst case at largest bandwidth, the SNR can be as low as 9.7dB at OSR of 24 due to increased distortion of ADC at high sampling frequency as shown in Fig. 7.16. It corresponds to a BER of 2.4×10^{-3} for FM0 ASK data.

(a) (b)

Fig. 7.29 FPGA prototype (a) board (b) testing setup

7.7 Measurement of the Reader with Tag

The basic measurement setup of reader with the developed tag is shown in Fig. 7.30. Two single-ended antennas are utilized to maximize the isolation α to be about 34dB between RX and TX. External PA is also utilized to generate desired output power.

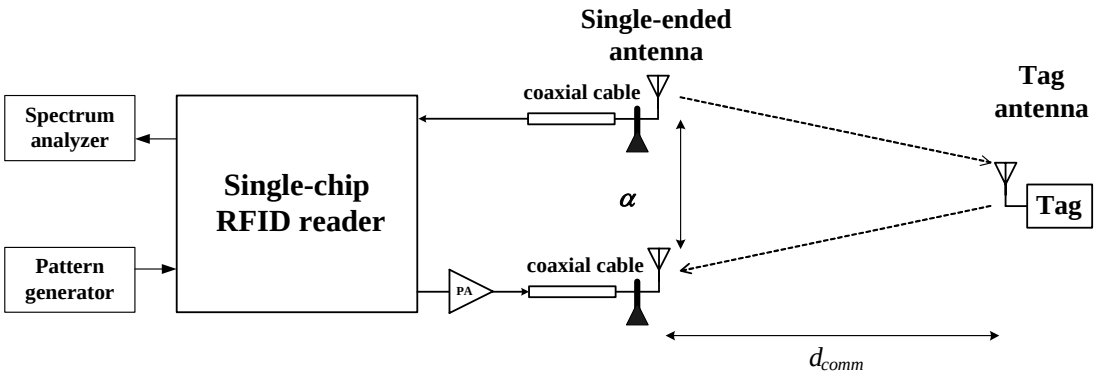


Fig. 7.30 Simplified testing setup of reader and tag

First, the reader to tag communication link is demonstrated by transmitting a 1W continuous wave and observing the clock output of tag's clock generator as shown in Fig. 7.31 and output DC voltage of the tag's rectifier. Then the tag to reader communication link is tested by measuring the CSF output spectrum. However, the communication distance d_{comm} is only about 1 meter. The main problem is due to the unexpectedly large leakage current of the circuits in the tag, which significantly increase the tag's power consumption and limit the communication distance. Besides, the complete system performance is quite sensitive to the environment influence, such as other nearby signals, metal reflections, antenna orientations, etc. These issues remain to be critical in practical RFID system implementations. For the reader, to enhance the performance, the noise floor of the TX should be further reduced to make sure the RX sensitivity doesn't dominate the communication distance, and the linearity of the RX should be improved to avoid gain suppression in the presence of

the large self-interferer.

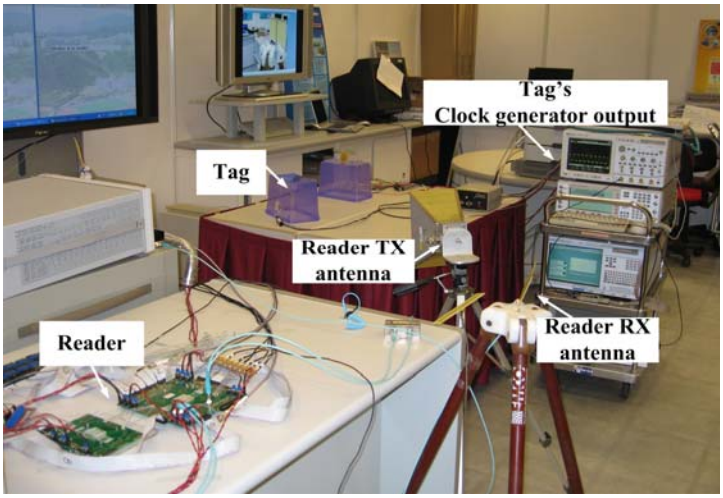


Fig. 7.31 Real testing setup of the reader and tag

Chapter 8
CONCLUSION

8.1 Key Features of the Proposed UHF RFID Reader

Though not without issues and challenges, RFID is a promising technology which analysts expect to become ubiquitous in the coming years, helping organizations solve problems in supply chain management, security, personal identification and asset tracking. Existing readers built from discrete components are bulky, power hungry and expensive. In this thesis dissertation, the feasibility of design and integration of a CMOS UHF RFID reader is demonstrated. High level of integration and less expensive CMOS technologies with less power consumption help to bring down the total cost of the RFID system implementation.

In addition to a number of issues related to the integrated radio transceivers, particularly in the context of CMOS technologies, the large self-interferer located in the center of the receiving band proves to be the most problematic to handle because it results in a dynamic range as large as 80dB at the receiver input. In chapter 2, the system was carefully studied. To avoid off-chip components, particularly passive IF filters, a dual-conversion zero-IF transceiver architecture is adopted which makes use of the DC-free coding scheme of the EPC Gen-2 specification. By doing this, not only the complete integration of the receiver signal path can be realized but also the

self-interferer is down-converted to DC which can be removed by DC offset cancellation.

The effects of the self-interferer on the RX performance are two-folds: saturation of the RX front-end and degradation of the RX sensitivity. To minimize the noise floor of the self-interferer, hence improve the reader RX sensitivity, the phase noise of the frequency synthesizer is the most critical. Due to the lack of high quality factor on-chip passive elements and lossy silicon substrate, the noise performance of the on-chip synthesizer is usually quite limited. In chapter 3, the modified transformer feedback VCO which exhibits enhanced tank Q and benefits from even harmonics noise filtering is presented. A 3rd-order single-loop $\Sigma\Delta$ modulator is optimized for the synthesizer in terms of phase noise and power.

With the goal of minimum power consumption in mind, the reconfigurable baseband architecture is described in detail in chapter 4. Three filters: active trap, continuous-time anti-aliasing filter and discrete-time channel selection filter are designed. The baseband features a tunable system bandwidth, tunable gain and high linearity. Theoretical analysis of the power optimization strategy subject to the constraint on noise and speed is presented in chapter 6. Our analysis leads to following conclusions: 1) for a given bandwidth and interference scenario, there is an optimal allocation of filtering and ADC resolution; 2) for a given interference rejection requirement, filter order and ADC dynamic range, the power increases almost linearly with the signal bandwidth.

In chapter 5, the other building blocks of the RFID reader are highlighted. To deal

with the self-interferer, the linearity of RX front-end needs to be sufficient and only limited gain can be afforded. A linearization technique utilizing 2^{nd}-order intermodulation injection is proposed in the LNA which suppresses the IM3 by 8dB. In the down-mixer, the current-mode interfacing of the two-stage mixer achieves the balance of linearity, noise and gain. The 4^{th}-order MASH 2-1-1 $\Sigma\Delta$ ADC is a key element for the reconfigurable baseband architecture. In the transmitter, the DAC exhibits superior linearity with very little power consumption. Linearity of the up-mixer is of primary concern so similar current-mode interface in the down-mixer is adopted. The two-stage class-A RF-VGA is optimized for linearity, output power and power efficiency. Finally the digital baseband is also briefly described.

Combing the system and circuit concepts developed, a complete RFID reader was presented in chapter 7 that integrates all the building blocks including the RF transceiver, IQ data converters and a digital baseband. It dissipates a maximum power of 249mW when transmitting maximum output power of 10.4dBm and receiving the tag's response of –70dBm in the presence of –5dBm self-interferer.

Table 8.1 compares the proposed reader with the other recently developed single-chip readers. All the reference works live with the self-interferer and adopt similar strategies as proposed in this work: zero-IF architecture to remove the down-converted self-interferer, high linearity RX front-end with limited gain to avoid saturation, synthesizer with low phase noise and attempt to maximize the isolation between RX and TX. This work achieves comparable performance with the CMOS implementation in [2], but focuses more on multi-protocol operation and

reconfigurability.

Table 8.1 Performance comparison of single-chip RFID readers

	[1]	[2]	This work
Process	0.18μm SiGe BiCMOS	0.18μm CMOS	0.18μm CMOS
Integration level	RF, BB for physical layer	RF, BB modem, MPU, memory	RF, BB
LO phase noise	-116@200kHz -144@3.6MHz	-87@100kHz -120@1MHz	-110@200kHz -127@1MHz
RX front-end P-1dB	11dBm	8dBm	3.5dBm
Sensitivity w/o self-interferer	-96dBm	N/A	-90dBm
Sensitivity w/ self-interferer	-78dBm @0dBm	-70dBm @0dBm	-70dBm@ -5dBm
Output power	20dBm	4dBm	10.4dBm
Die size	$21mm^2$	$23.9mm^2$	$18.3mm^2$
Total power	1.5W	160mW	249mW

8.2 Contributions of the dissertation

First, the simultaneous transmitting and receiving makes the design of the RFID reader more challenging than conventional wireless transceivers. The effects on the RFID reader due to the self-interferer are studied and analyzed thoroughly. Measures to deal with the self-interferer are proposed in the system level and circuit level which proves to be feasible and effective. RX operations are separated into listen mode and talk mode with different design focuses.

Then, the reader specification is derived based on careful study and investigation of different regulation documents, in the absence of any available literature work of RFID reader design. In particular, a multi-protocol reader concept is proposed that is able to dynamically minimize the power consumption while meeting all the

multiple-protocol requirements in terms of data rates and dynamic range.

A low-voltage low-power fractional-N frequency synthesizer is proposed. The TF-VCO is modified from the original design to achieve optimal phase noise performance under low supply voltage. The ΣΔ modulator is proposed based on careful consideration of all the noise and power issues related to ΣΔ fractional-N frequency synthesizer. The power and noise optimization in a fractional-N frequency synthesizer are addressed in detail. The synthesizer achieves comparable noise performance but consumes less than 5mW total power which is much lower than the other state-of-the-art work.

Propose a systematic design and optimization methodology for the reconfigurable mixed-signal baseband with sufficient verification and measurement. Theoretical analysis is performed which proves in the system level an optimal distribution of analog channel selection filtering and ADC dynamic range exist for a given baseband speed and interference. It can be a guideline in the choice of baseband architecture, clock frequency of the filter and ADC, the filter order, and modulator parameters. It also illustrates that the power of the proposed mixed-signal baseband is linearly proportional to signal bandwidth, just like a pure digital circuits. In the circuit level, a tunable active trap is proposed to attenuate interference at different offset frequencies since the proposed reader has a variable bandwidth. 12dB notch at alternate adjacent channel improves the receiver IIP3 by 8dB. The AAF and CSF are designed and optimized for the target system requirement. Discrete tuning mechanism are proposed for all the bandwidth tuning which not only provides large tuning range but

also forms an easy interface between digital control blocks and analog circuit without the need for further D/A or A/D conversion.

Finally, the integration of various building blocks is performed, which involves significant complexity. The RX performance including the effects of self-interferer and reconfigurability is fully characterized. The TX performance from DAC to PA is also measured. The TRX can meet the targeted requirement. In addition, the TRX is measured with digital baseband. Finally, the basic communication between reader and tag is also demonstrated.

In conclusion, a single-chip CMOS UHF reader is successfully implemented that achieve comparable performance with the state-of-the-art design.

8.3 Recommendations for Future Work

There are a number of issues that await exploration in the future research studies. In particular, the ability to handle large self-interferer remains a big challenge in reader implementation. Not only the self-interferer but also its noise floor should be rejected to improve the sensitivity and linearity of the receiver. Ideally, the filtering should be performed at RF frequency to relax the performance of the RX front-end circuits. Novel circuit techniques are required which effectively cancel the interferer but keep the desired signal unaffected. High selectivity (Q~2000) passive filters can definitely help, but they are not available in the present microwave technology. Recently on-chip Nano-Electro-Mechanical (NEMs) and Micro-Electro-Mechanical (MEMs) filters have received great attention for the replacement of SAW filters. These filters can take very small die size and can potentially be integrated on the same silicon chip.

Quality factor as high as 10000 are already demonstrated in the GHz frequency region [3]-[7]. With such high selectivity low loss filter, the succeeding electronic blocks in the receiver no longer need to handle the interferers, which implies remarkable power saving.

However, before the technologies mature, most RFID readers still have to live with the self-interferer. The linearity of the front-end needs further improvement to handle larger than 0dBm self-interferer. For high linearity purpose, high supply voltage design with thick oxide device might be a suitable choice at the cost of larger power consumption and large parasitic capacitance. Besides, the synthesizer should be designed with even lower phase noise to reduce the noise induced by the self-interferer. Unfortunately, the lack of high-Q inductor and transformer presents a fundamental limitation to the phase noise of the fully-integrated frequency synthesizer. It is possible to design VCO at a higher frequency, for example, 4×LO1 (about 2.4GHz) or even 8×LO1 (about 4.8GHz), so that after more dividers, LO1 phase noise can be improved. The isolation of the RX and TX can be improved to remedy the issues caused by the self-interferer.

Although some work has been done on the power optimized baseband architecture with its validity proved mathematically, the analysis still limits to quite ideal case. For example, finite gain and bandwidth of the opamps are neglected, phase noise of the interferer are neglected, etc. As a result, the power, filter attenuation requirement and ADC dynamic range are all more or less under-estimated.

Moreover, the tuning of the analog bias current and the decision of bypassing the

CSF or not are controlled manually in the prototype. For a complete solution, some intelligent and systematic ways are needed. To reconfigure for different interference, it is possible that multiple RSSIs are implemented before and after the CSF to determine whether a received signal strength is dominated by an out-of-band interference signal or by an in-band desired signal. For example, if the filter RSSI output voltage is smaller than the one at filter input, this will be an indication that the large incoming signal is due to an out-of-band interference [8]. Based on this determination, the filter can be decided to be bypassed or not. Since reader determines the communication data rate, the clock frequency, AAF and active trap bandwidth control bits and analog bias current of the CSF and ADC can also be defined to reconfigure the baseband. For the transmitter, to support multiple standards, output power of RF-VGA can be tuned by gain control bits. The choice of SSB-ASK and DSB-ASK is determined by the baseband input signal as shown in Fig. 2.21.

Another area that needs further investigation is the subject of substrate noise coupling in integrated radio systems. There is a strong need but also a lack of the model for noise coupling mechanisms in mixed-signal system due to the extreme complexities involved. Design techniques that can mitigate or reduce interference between digital and radio blocks are desired.

In the future, process scaling may necessitate a reduction in supply voltage for integrated transceivers. This trend presents a number of challenges for high dynamic range system design. Thus, an investigation into low-voltage radio techniques would

also be an interesting and essential topic.

Finally, to completely characterize the performance of the reader transceiver, the demonstrations of reader transceiver with digital baseband and reader with tag are necessary. Moreover, the influence of the environment on the communication distance should also be measured to gain more insight into the limitations of the passive RFID systems.

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